EPLD

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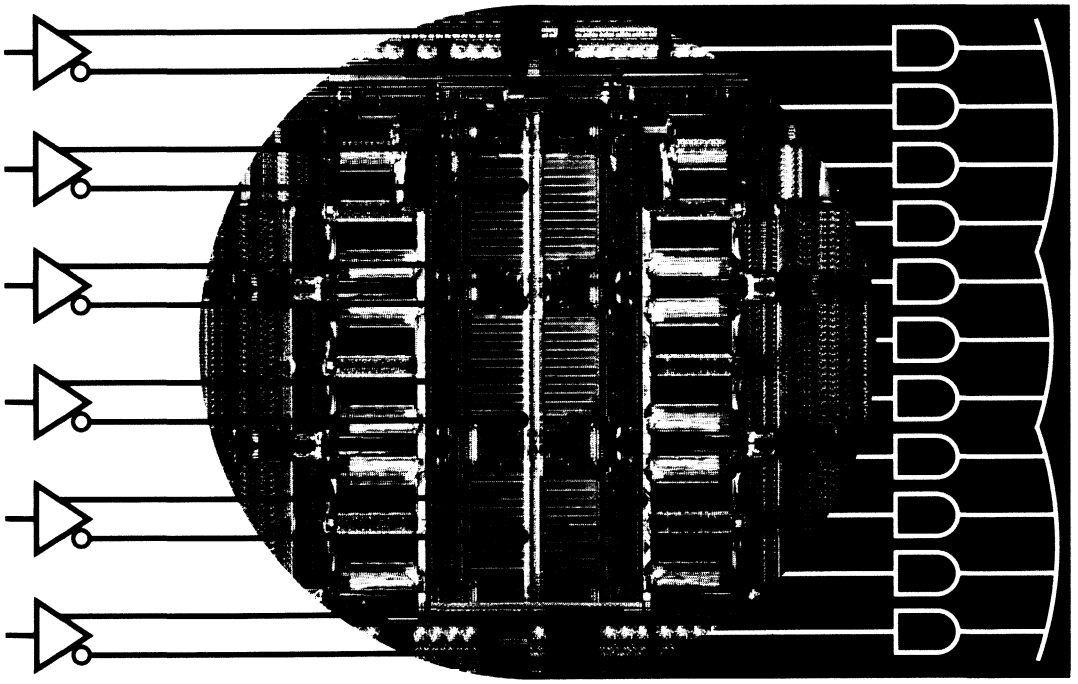
PAL Conversion Guide With Xilinx EPLD Data Sheets



August 1993

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Xilinx EPLDs
The Best Solution for PAL® Conversion

Welcome and thanks for your interest in Xilinx EPLD products.

If you're like most PAL designers, you're interested in converting your designs to more complex devices like Xilinx XC7200/A and XC7300 EPLDs. But you're probably also a bit skeptical about the different claims vendors have made about their products. The PAL Conversion Guide will help you better understand how PAL conversion is accomplished with Xilinx EPLD products.

PAL conversion vs. PAL integration.
The typical design requirement is PAL conversion, but most products on the market today address PAL integration. The semantics here are very important. Any high pin-count logic device can ***integrate*** multiple PALs into a single device. But complex programmable logic devices, like FPGAs, differ architecturally from the simple array structures of PALs. This means that PAL integration works only after a lot of time and effort is spent in redesign. Even complex product term-based products can pose significant barriers to the integration process.

Xilinx offers the first *true* PAL conversion process.
The Xilinx PAL conversion process allows you to take the original source files for your PAL or GAL based design, and directly convert it to either XC7200/A or XC7300 EPLDs, without redesign. Designs can be converted quickly and easily, with virtually no risk. If you use ABEL™, PALASM™ or CUPL™, it's no problem. You can easily convert designs done with these tools to a working XC7200/A or XC7300 device. The XC7300 family's unique Dual Block™ architecture, along with the PAL conversion utilities contained in the Xilinx EPLD software, make it easy.

The Dual Block architecture incorporates two types of logic blocks on each device. One type is optimized for simple PAL functions that require high pin-to-pin speed, and the other type is optimized for product-term-rich PAL or GAL functions that require high clock cycle rates. Unlike other CPLDs, Xilinx devices are FAST and COMPLEX. This allows individual PAL devices to be mapped directly to the appropriate logic, and connected just as they appear on the PCB.

Please take a few minutes to look over the Xilinx PAL Conversion Guide. We believe you'll agree that Xilinx EPLDs provide ***the best solution for PAL conversion.***

EPLD Product Marketing

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SECTION TITLES

XILINX®

SECTION 1

New, Enhanced

XILINX

EPLD Products

The BEST Solution

for PAL Conversions

Dual Block™ EPLD

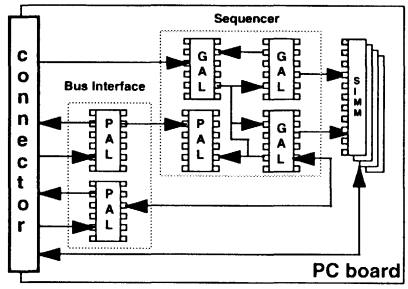
Direct PAL Conversion Without Redesign

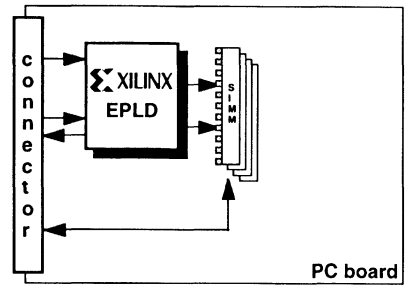
The Old Way:

- Fast PALs
- Complex GALs
- Large PC boards

The New Way:

- XC7200/7300 EPLD Family
- Predictable performance
- 100% interconnect on-chip





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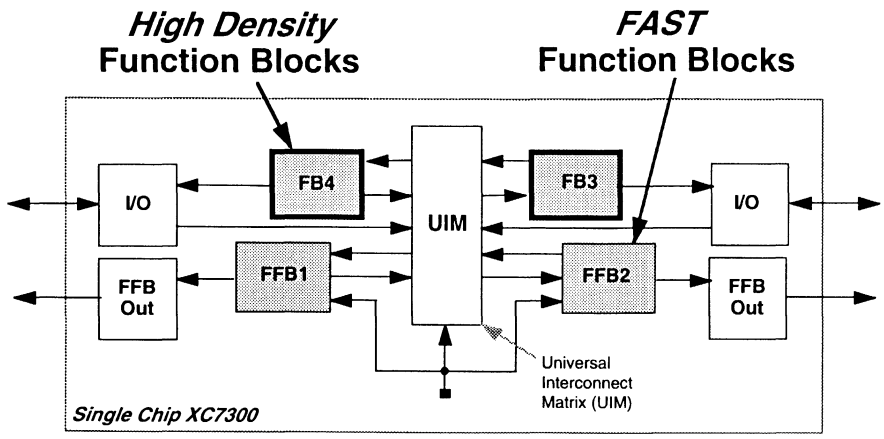
Dual Block™ EPLD

XC7300 Dual Block™ Architecture

The Fast and Complex Advantage



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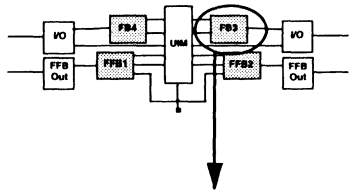
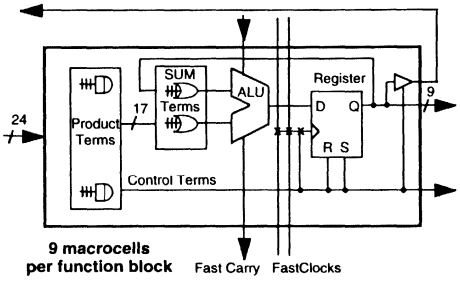
Dual Block™ EPLD

XC7000 High Density Function Block

Features

- ✔ Built-in ALU and fast carry
- ✔ Complex logic capability
  Equivalent to a 22v10 PAL
- ✔ 3 Sync/async clock options





Performance

- ✔ 60 MHz state machines
  Guaranteed across the chip
- ✔ n-bit counters run at 60 MHz
  Independent of length
- ✔ 40 MHz, 18 bit accumulators

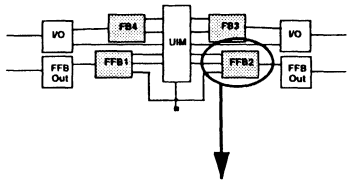
XILINX

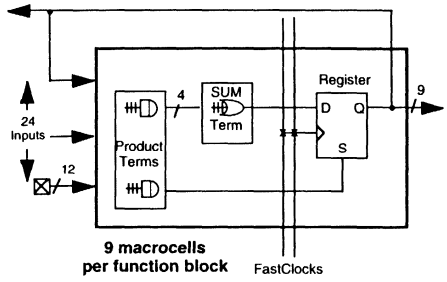
Dual Block™ EPLD

XC7300 Fast Function Block

Features

- ✔ Optimized for performance
  Simplifies high speed path design
- ✔ 12 high speed direct inputs
- ✔ 2 synchronous clock options





Performance

- ✔ 100 MHz maximum clock rate
- ✔ 10 ns pin-to-pin t_{PD}
- ✔ 8 ns clock-to-out t_{CO}

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Dual Block™ EPLD

Easy-to-Use PAL Conversion Software

Supports Industry-Standard Tools & Interfaces

PAL COMPILER
ABEL, Cupl

SCHEMATIC EDITOR
OrCAD, Viewlogic

TEXT EDITOR

Xilinx XACT® PAL Fitter

XEPLD TRANSLATOR
DS550

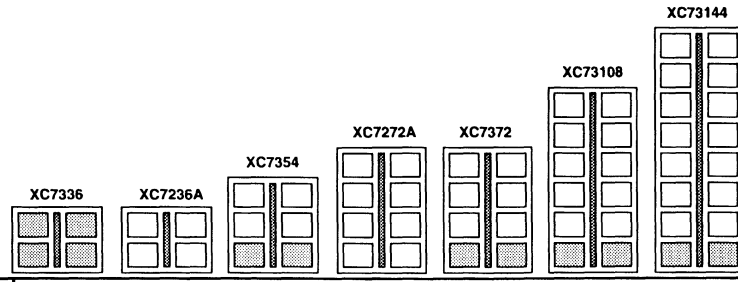
PAL Files to a Programmed EPLD in Minutes!

DEVICE PROGRAMMER
HW120

XILINX

Dual Block™ EPLD

Broad Range of XC7000 Products



Equiv. PALs	**3-4**	**4**	**6**	**8**	**8**	**12**	**16**
Registers	36	68	108	126	126	198	234
t_{PD}	7.5 ns	25 ns	10 ns	25 ns	10 ns	12 ns	10 ns
f_{CYC}	110 MHz	60 MHz	100 MHz	60 MHz	100 MHz	80 MHz	100 MHz
Packages	44 PLCC	44 PLCC	44/68 PLCC	68/84 PLCC 84 PGA	68/84 PLCC 84 PGA	84 PLCC 144 PGA 160PQFP	184 PGA

☐ High-Density FB ▨ FAST FB

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SECTION 2

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Direct PAL Conversion Using Xilinx EPLDs

Direct PAL Conversion Using Xilinx EPLDs

BY JEFFREY GOLDBERG

Introduction

In order to remain competitive in the marketplace, companies are being driven to reduce product manufacturing costs while adding more features and improving reliability. Users of low density discrete PALs are turning to higher density erasable programmable logic devices (EPLDs) to meet these goals.

PALs are easy devices to use. Device timing is fixed, routing issues are nonexistent and the device architectures are simple and understandable. Many EPLDs however, exhibit timing unpredictability, routing limitations, and limited functionality that can trap the unwary first-time EPLD user. Couple that with the task of learning how to use new design-entry software, and what appeared to be a simple task can turn into a nightmare.

This application note shows how Xilinx EPLDs can be used to simplify the task of reducing the number of discrete low density PALs on a board. This direct PAL conversion is made possible by a unique combination of :

- Architectural features
- Software methodology
- Broad product family

Xilinx EPLD Architecture

In order to support direct PAL conversion, Xilinx EPLDs have a PAL-like architecture. Each device consists of several PAL-like logic blocks, called Function Blocks (FBs), on a single IC, all interconnected by a fully populated switch matrix. Each FB can be thought of as a 21V9 PAL, with 21 complementary inputs and an AND-OR array with 57 product terms feeding 9 outputs.

The Xilinx EPLD Function Block is highly flexible superset of the low density PAL. The product term intensive FB has five individual product terms per output. In addition, there are 12 product terms that are shared between all 9 outputs. Each output can be configured as either registered or combinatorial. Each register has individual set, reset and output enable control and can be clocked either individually or by global clocks. In addition, each output has an available XOR gate that can be used for XOR functions or toggle flip flop emulation.

Although product-term-intensive, the timing is fixed. No matter whether the output is performing a single product-term function or a 17 product-term function with the XOR gate, the timing doesn't change. Just like a PAL.

All of the Function Blocks on a Xilinx EPLD are interconnected by a fully populated Universal Interconnect Matrix (UIM™).

Unlike other vendor's sparsely populated matrices that create routing problems and have fanout-dependent timing, the UIM is a fully populated, non-blocking switch matrix that features a constant delay, independent of fanout. Every Function Block output and every signal from every input and I/O pin all feed into the UIM. The UIM in turn drives every input of every FB. This means that each Function Block input can be driven by any input pin, any I/O pin and any Function Block output – just like connecting PALs on a board, but better.

In addition to serving as an interconnect, the UIM may also function as very wide input AND array. This allows the EPLD to generate product terms in the UIM – just like a low density PAL AND array. And like a PAL, propagation delay is fixed regardless of the number of signals used to generate the product term, or the source and destination of those signals.

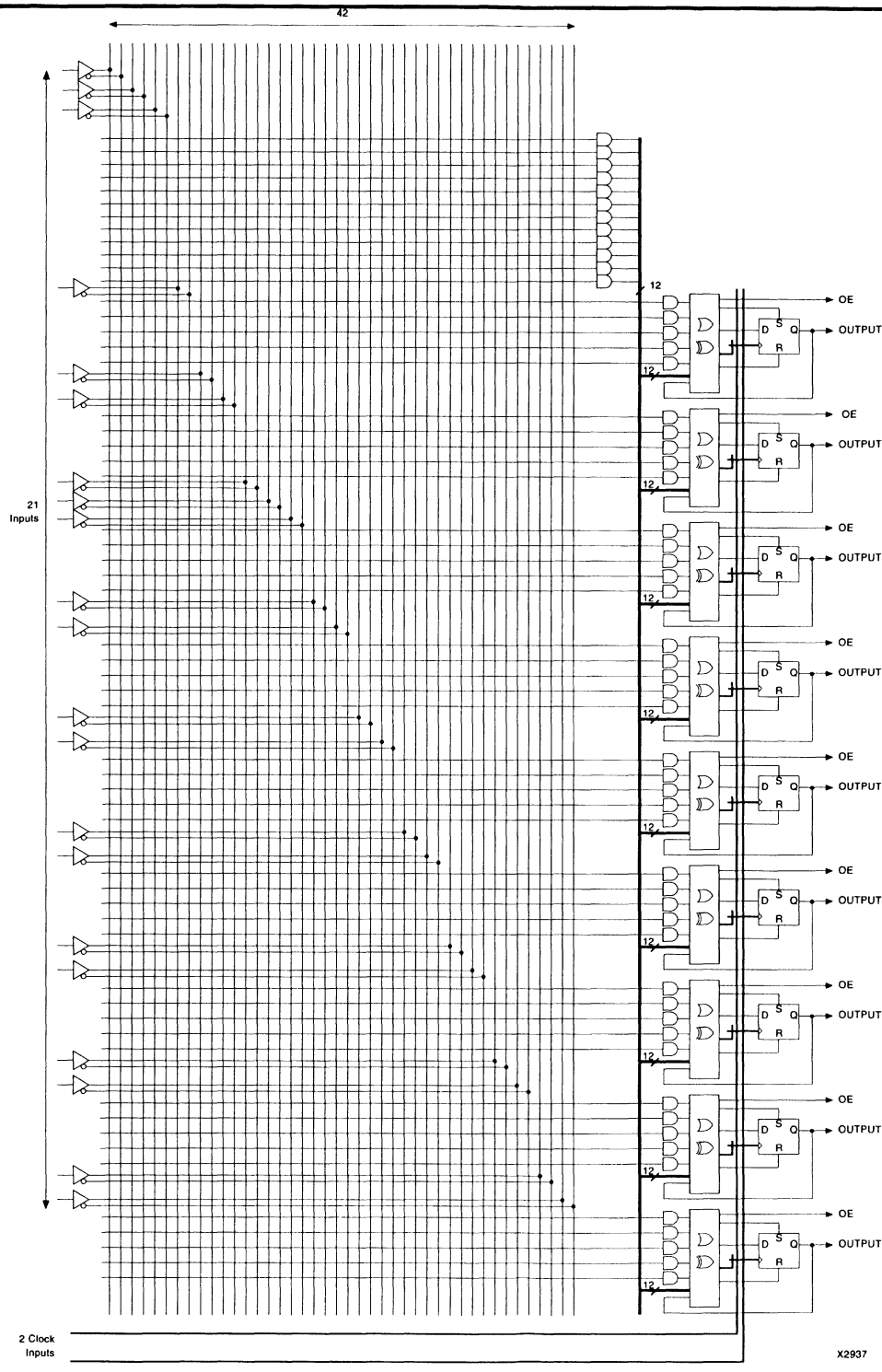


Figure 1. Xilinx EPLD PAL-Like Function Block

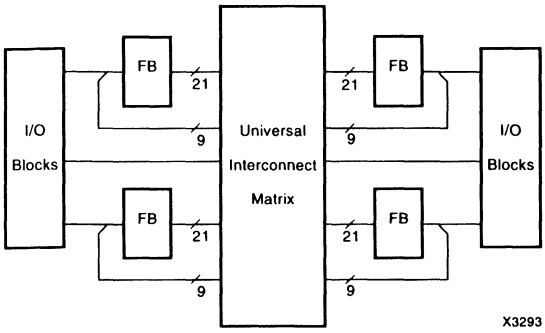


Figure 2. Universal Interconnect Matrix

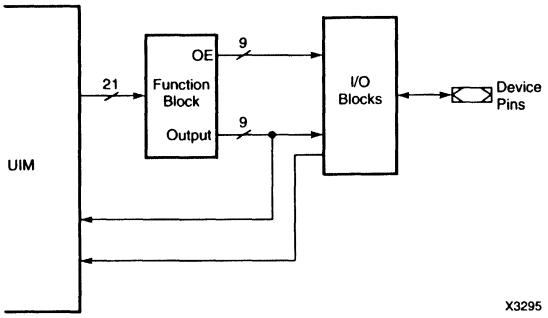


Figure 4. I/O Block

The EPLD has programmable I/O blocks for driving the device pins. The I/O blocks can be used to decouple the Function Block's outputs from the device pins so the Function Block outputs may be buried while still retaining the use of the pin as a device input. The I/O blocks also provide output inversion control and the ability to latch and register input signals.

Xilinx EPLD Software

When it comes to programmable logic, silicon is only part of the solution. Software is required to translate ideas into reality. The Xilinx EPLD Translator (XEPLD™) works with industry standard PAL logic compilers and languages such as ABEL, CUPL and PALASM. One can directly import JEDEC files from old, proven designs using 22V10s and 20V8s.

The bottom line - the XEPLD system allows design entry with familiar front end tools. Once the design is entered, XEPLD simply acts as a fitter, taking the design description and mapping it into the chosen Xilinx EPLD.

In addition to being easy to use, XEPLD is very powerful. One of the most important functions of a fitter for high density programmable logic is Automatic Partitioning. The design can be entered without having to first partition it into Function Block-size pieces. This lets the designer concentrate on the functionality of the design, not its physical implementation.

The PAL Conversion Process

The PAL conversion process is begun by identifying which group of PALs are to be converted to a single EPLD. Then choose the appropriate Xilinx EPLD, based on the I/O and logic requirements. Xilinx makes this process easier by offering each device in a variety of footprint-compatible packages. This flexibility allows the designer to upgrade to a higher density device without having to change the board layout, should the logic requirements change.

Since the timing of the Xilinx EPLD is absolutely predictable, it is an easy matter to verify that the design will meet all critical timing requirements. By eliminating delays getting on and off chip, even D series PALs can be converted to a single Xilinx EPLD.

The choice of whether to do equation-based design entry or schematic-based design entry is based primarily on the user's preference. Equation-based entry allows the user to concatenate PALASM equations from multiple PAL files without any restrictions on the PAL type. Equation-based entry gives the user more control over how the logic is mapped into the EPLD.

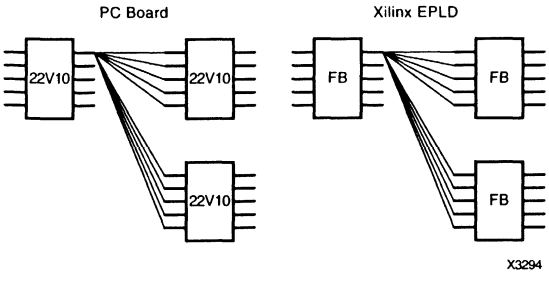


Figure 3. The 100% Interconnect

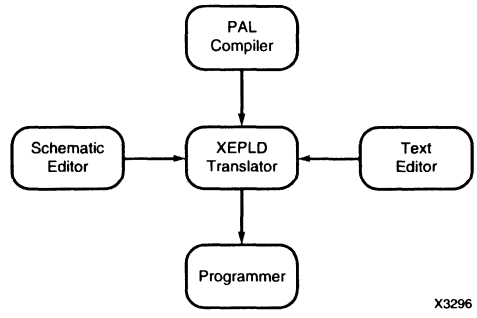


Figure 5. Development System Overview

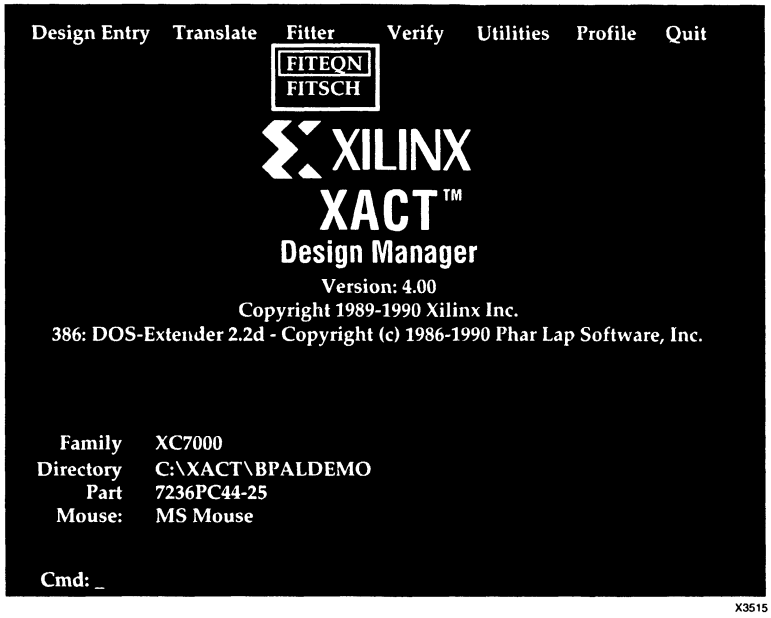


Figure 6. XEPLD Runs Under the Xilinx Design Manager

On the other hand, schematic-based design entry may be easier to conceptualize, and it allows the user to directly import JEDEC files for 22V10 and 20V8 PALs (PALASM equations may be used for other PAL types).

The following examples show how to use XEPLD to directly convert a multiple-PAL design to a single Xilinx EPLD. The examples show the use of both equation and schematic-based design entry methods. The design, shown in Figure 7, implements a UART originally implemented with two 22V10s, a 20V8 and a single 20RA10.

Direct PAL conversion implies that there is absolutely no redesign necessary to convert the design to a single Xilinx EPLD. The reader, therefore, needs to be aware of two issues that may affect a design's suitability for direct conversion.

1. Designs implemented with XOR PALs such as the 20X10A series require minor syntax changes in their PALASM output files to conform to how XOR operations are expressed for Xilinx EPLDs.
2. Because asynchronous presets and resets function differently in different PALs, the architectures of the original PAL and the Xilinx EPLD need to be considered when converting the design. In the Xilinx EPLD architecture, inversions are performed before the register, not after the register output. If the original PAL performed the inversion after the register, (e.g. a 20RA10), its output pin goes HIGH when the register is reset, whereas the Xilinx EPLD Function Block output would go LOW. A simple modification to the PAL's source code before generating the PALASM file may be all that is required (e.g. changing the reset to a preset).

Equation-Based Design Entry

Direct PAL conversion is easily accomplished with a modular design approach. Each PAL in the design can be treated as an individual module. A top level design file simply links all of the modules together. Since this file need only contain declaration statements that manage the design (e.g. define the chip's inputs and outputs), it is created with a minimum of effort. XEPLD reads the top level file, concatenates the equations for each individual PAL, automatically partitions the equations and converts the multiple-PAL design to a single chip solution. This design flow is illustrated in Figure 8.

For each PAL in the design, generate a PALASM Boolean equation file from the original PAL source code. This is easily done with the ABEL XFER utility or the CUPL -c compiler option. At this time, verify that the signal names in each PAL pinlist establishes the proper signal connectivity for the design.

Using a text editor, write the top level design file. The design file PAL_UART.PLD, shown in Figure 9, was created for the UART design. This file is written in PLUSASM, the XEPLD native syntax, and should look very familiar to those familiar with PALASM.

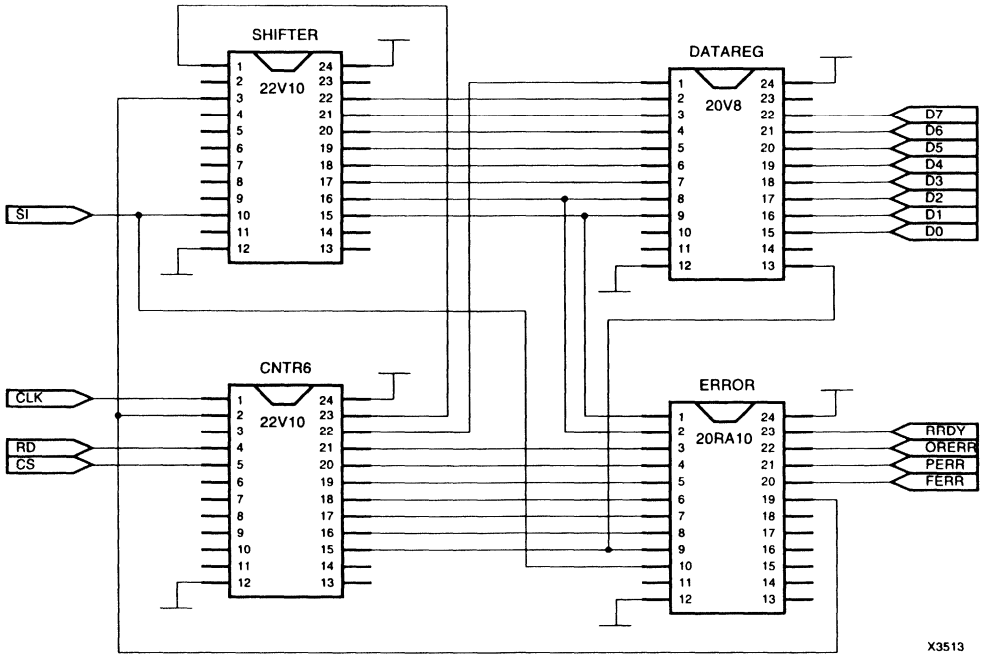


Figure 7. Original UART Design

Like PALASM, this file begins with a title block for design documentation, followed by INCLUDE_EQN keywords that instruct XEPLD to concatenate the PALASM equations contained in each of the included files that were generated by the PAL compiler.

The CHIP statement contains the filename of the top level file (without the file extension) and targets a Xilinx EPLD.

INPUTPIN, OUTPUTPIN and NODE keywords then follow to define the devices inputs, outputs and nodes. This is followed by the FASTCLOCK keyword that assigns signals to the global FastClock lines.

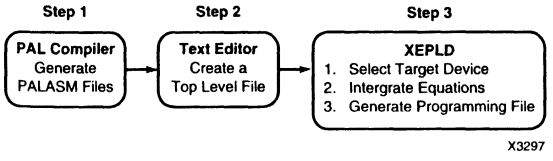


Figure 8. Equation-Based Design Flow

The EQUATIONS keyword indicates where the equations section of the design file begins. After reading this keyword, XEPLD reads all of the equations in the included files.

After completing the top level design file, do the following:

- Select the target device:

  Open up the FAMILY menu and select the XC7000 device family. Then open up the PART menu and select the target Xilinx EPLD.

- Integrate the equations:

  Open up the FITTER menu and select FITEQN, then PAL_UART.PLD. XEPLD then processes the design to create the database file PAL_UART.VMH.

- Generate the device programming file:

  Open up the VERIFY menu and select MAKEPRG, then PAL_UART.VMH. Assign the signature, PALUART.A, and XEPLD will now produce the device programming file, PAL_UART.PRG.

The device can now be programmed and the correct system operation verified.

```
TITLE          TOP LEVEL DESIGN FILE FOR PAL_UART
AUTHOR         EPLD APPLICATIONS
COMPANY        XILINX
DATE           2/3/93

INCLUDE_EQN    'SHIFTER.PDS'
INCLUDE_EQN    'CNTR6.PDS'
INCLUDE_EQN    'DATAREG.PDS'
INCLUDE_EQN    'ERROR.PDS'

CHIP           PAL_UART XEPLD

INPUTPIN       SI RD CS

OUTPUTPIN      D0 D1 D2 D3 D4 D5 D6 D7 RRDY ORERR PERR FERR

NODE           S0 S1 S2 S3 S4 S5 S6 S7 EN Q0 Q1 Q2 Q3 Q4 Q5 DATACLK SHIFTCLK
               PAR START

FASTCLOCK      CLK

EQUATIONS
```

Figure 9. Top-Level Design File

Schematic-Based Design Entry

The schematic design entry flow is also simple and straightforward. The XEPLD component library contains 22V10 and 20V8 PALs to simplify the PAL conversion process. It is a simple matter to connect the PALs exactly as in the original design and import JEDEC files that describe their functionality. For other PAL types such as the 20RA10 used in the original design, PALASM equation files can be used instead. XEPLD then processes the netlist and PAL files to convert the design to a single chip solution. This design flow is illustrated in Figure 10.

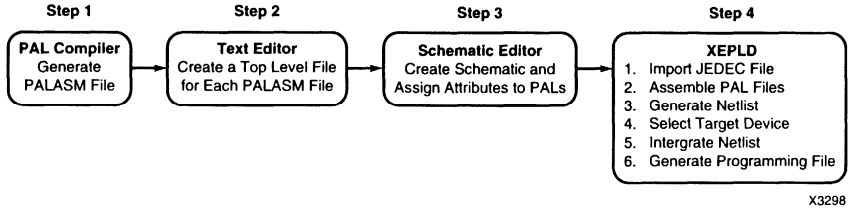


Figure 10. Schematic-Based Design Flow

For each 22V10 and 20V8 in the original design, use the existing JEDEC files generated by the PAL compiler. For other PAL types, generate a PALASM Boolean equation file. Then, using a text editor, create a top level file for each PAL that a PALASM equation file was created for. This file is similar to the top level design file for the equation based design entry, with two differences:

1. The CHIP statement targets the PAL in the schematic, not a Xilinx EPLD
2. A pinlist is used to define the pinout of the PAL in the schematic

Any PAL in the XEPLD component library that meets the I/O requirement can serve as the target device, but the PL22V10, PL20V8 and PLFPLA48 are recommended to take advantage of the automatic partitioner.

In this design example, a PL22V10 was chosen as the target device for the ERROR PAL, even though a 20RA10 was used in the original design. This is permitted because both the PL22V10 and PL20V8 library components have the full functionality of the Xilinx EPLD architecture and do not suffer the architectural limitations of the discrete devices they replace. The top level file, ERROR.PLD is shown in Figure 11. Note that each pin position must have either a signal name or a no-connect (NC) assigned to it.

Now use the schematic editor to capture the design. Assign an attribute to each PAL in the schematic that links the PAL to an intermediate file that describes it's function. In Viewlogic, the attribute @PLD=<file_name> is assigned with the ViewDraw attribute command. When using OrCAD, edit the PAL's partfield to read PLPLD=<file_name>. Save the design file when done.

```
        TITLE           TOP LEVEL DESIGN FILE FOR ERROR DETECTOR PAL IN PAL_UART DESIGN
        AUTHOR          EPLD APPLICATIONS
        COMPANY         XILINX
        DATE            2/3/93

        INCLUDE_EQN     'ERROR.PDS'

        CHIP            ERROR PL22V10

;   1   2   3   4   5   6   7   8   9   10   11   12
    S0  S1  Q5  Q4  Q3  Q2  Q1  Q0  EN  SI   NC   GND
;   13  14  15  16  17  18   19      20     21     22      23     24
    NC  NC  NC  NC  NC  PAR  START  FERR  PERR  OREER  RRDY  VCC

    EQUATIONS
```

Figure 11. PLUSASM File ERROR.PLD

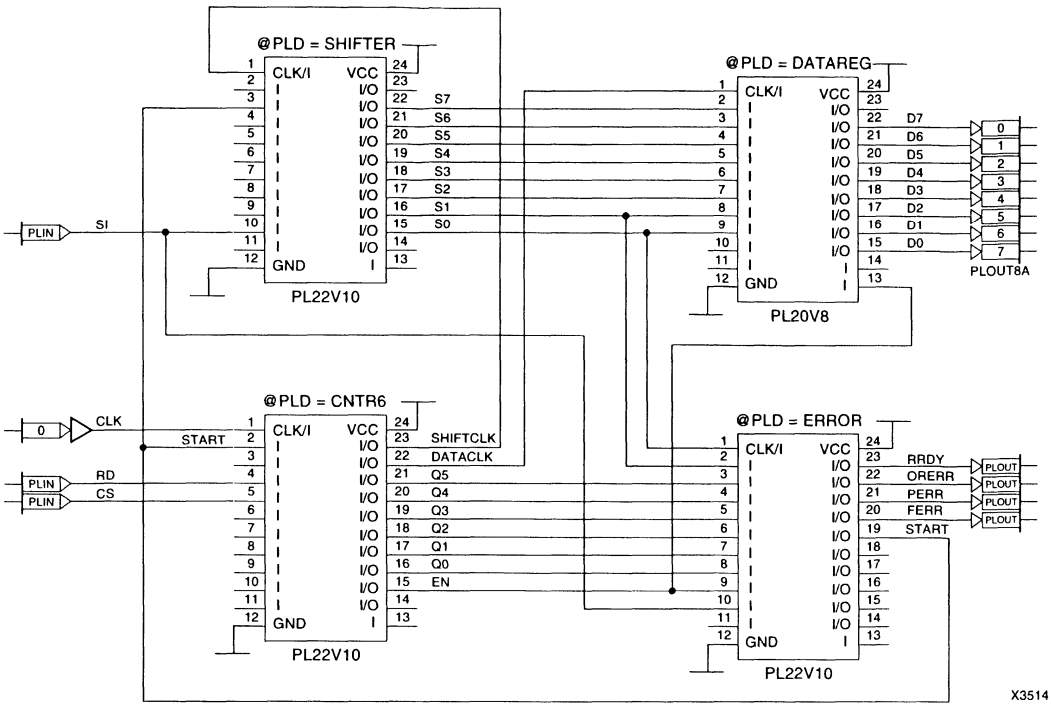


Figure 12. PAL_UART Workview Schematic

Now the design is ready to be processed.

Generate the netlist:
Open up the TRANSLATE menu and select WIR2NET, then PAL_UART.1 to generate a Viewlogic netlist. If the design was captured with OrCAD, select STD2NET instead, then PAL_UART.SCH to generate the OrCAD netlist.

Import a JEDEC file or Assemble the Equation File for each PAL in the schematic:

- To Import a JEDEC File:

  Open up the TRANSLATE menu and select JED2PLD, then SHIFTER.JED to import the JEDEC file. Type in the desired filename for the equation file that will describe the PAL's functionality, SHIFTER.PLD, then select the PAL type, PL22V10. XEPLD will automatically partition the logic into one or more Function Blocks and create the intermediate PAL description file SHIFTER.VMH. Repeat this procedure for each JEDEC file to be imported.

- To Assemble an Equation File:

  Open up the TRANSLATE menu and select PLUSASM, then ERROR.PLD to assemble the top level file for the PAL. Remember, XEPLD will reference the equations in the included PALASM file, ERROR.PDS. XEPLD will partition the logic and create the intermediate PAL description file ERROR.VMH.

Integrate the netlist:
Open up the FITTER menu and select FITNET, then PAL_UART.NET to integrate the netlist.

Generate the device programming file:
Open up the VERIFY menu and select MAKEPRG, then PAL_UART.VMH. Assign the signature, PALUART.A, and XEPLD will now produce the device programming file, PAL_UART.PRG.

The device can now be programmed, installed on the board and correct system operation verified.

Conclusion

This application note demonstrates how easy it is to directly convert PAL based designs to a single Xilinx EPLD without any redesign. This direct conversion process is only possible when the target device logic blocks have a PAL-like architecture, the interconnect matrix is fully populated and chip timing is completely independent of product term utilization and layout. The Xilinx EPLD Translator simplifies this task by interfacing directly to the third party design tools that the designer is already familiar with.

XILINX®

SECTION 3

XC7236/XC7236A
36 Macrocell CMOS EPLD

Preliminary Product Specifications

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 36 Macrocells, grouped into four Function Blocks, interconnected by a programmable Universal Interconnect Matrix (UIM)
- Each Function Block contains a programmable AND-array with up to 24 complementary inputs, providing up to 17 product terms per Macrocell
- Enhanced logic features
  - Arithmetic Logic Unit in each Macrocell
  - Dedicated fast carry network between Macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all Macrocell logic paths
- 36 signal pins
  - 30 I/Os, 2 inputs, 4 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ± 0.3 V
- Three high-speed, low-skew global clock inputs
- 44-pin plastic and windowed ceramic leaded chip carrier packages

General Description

The XC7236/A is a second-generation High Density Programmable Logic Device that combines the classical features of the PAL-like EPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output Macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each Macrocell. Dedicated fast arithmetic carry lines running directly between adjacent Macrocells and Function Blocks support fast adders, subtractors and comparators of any length up to 36 bits.

This additional ALU in each Macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent Macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and Macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Function Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 36 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7236/A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Automated design mapping is supported by Xilinx development software based on design capture using third-party schematic entry tools, PLD compilers or direct text-based equation files. Design mapping is completed in a few minutes on a PC.

Architectural Overview

Figure 1 shows the XC7236/A structure. Four Function Blocks (FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output Macrocells (MCs) that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macrocells drive a 3-state chip output; all feed back into the UIM.

The device also contains six dedicated FastCompare and FastDecode logic paths for address compare, decode or gating functions. The following pages describe the elements of this architecture in detail.

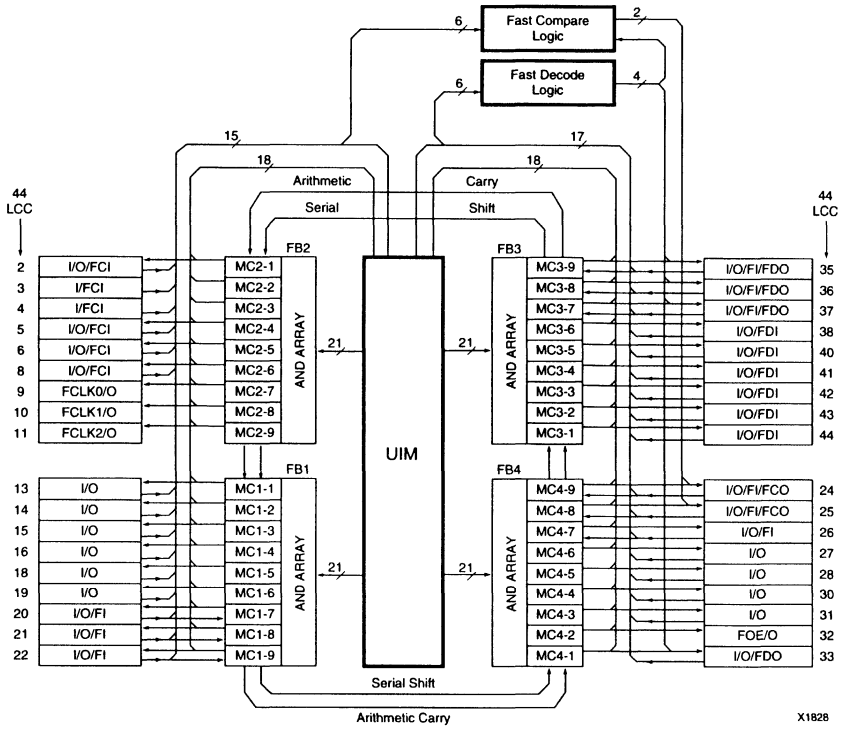


Figure 1. XC7236/A Architecture

Function Blocks and Macrocells

The XC7236/A contains 36 Macrocells with identical structure, grouped into four Function Blocks of nine Macrocells each. Each Macrocell is driven by product terms derived from a programmable AND array in the Function Block. The AND array in each Function Block receives 21 signals and their complements from the UIM. In three Function Blocks, the AND array receives three additional inputs and their complements directly from FastInput (FI) pins, thus offering faster logic paths.

Five product terms are private to each Macrocell; an additional 12 product terms are shared among the nine Macrocells in each Function Block. Four of the private product terms can be selectively ORed together with up to four of the shared product terms, and drive the D1 input to the ALU. The other input, D2, to the ALU is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms.

As a programmable option, four of the private product terms can be used for other purposes. One of the private product terms can be used as a dedicated clock for the flip-flop in the Macrocell. (See the subsequent description of other clocking options.) Another one of the private product terms can be the asynchronous active-High Reset of the Macrocell flip-flop, another one can be the asynchronous active-High Set of the Macrocell flip-flop, and another one can be the Output Enable signal.

As a configuration option, the Macrocell output can be fed back and ORed into the D2 input to the ALU after being ANDed with three of the shared product terms to implement counters and toggle flip-flops.

The ALU has two programmable modes: In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to max 17 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block in each Macrocell can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the next lower Macrocell. It also feeds a carry output to the next higher Macrocell. This carry propagation chain crosses the boundaries between Function Blocks. This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture, when trying to perform arithmetic functions.

The ALU output drives the D input of the Macrocell flip-flop. Each flip-flop has several programmable options. One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock. Otherwise, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable and is either the dedicated product term mentioned earlier, or one of two global FastCLK signals (FLCK0 or FLCK1) that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each Macrocell flip-flop can be preloaded with either 0 or 1.

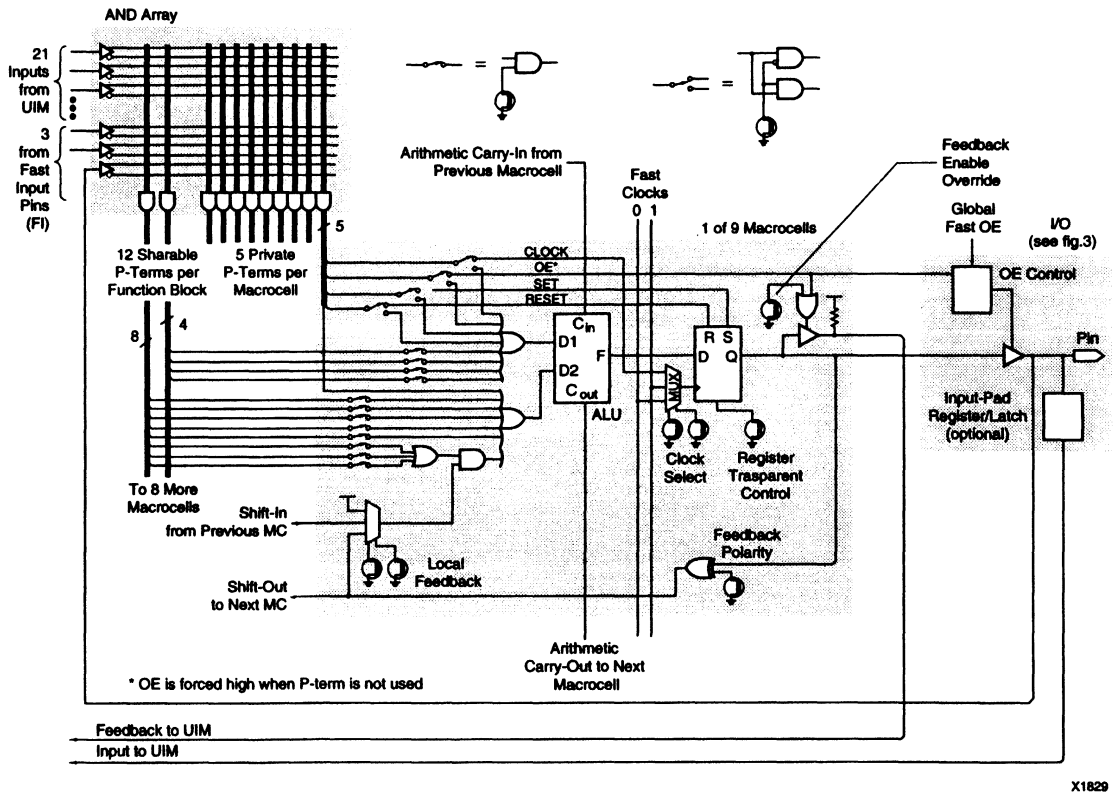


Figure 2. Function Block and Macrocell Schematic

In addition to driving a chip output pin, the Macrocell output is also routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output pin driver and/or the feedback to the UIM. If configured to control UIM feedback, then when the OE product-term is de-asserted, the UIM feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 68 inputs: 36 from the Macrocell feedbacks, 30 from bidirectional I/O pins, and 2 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 84 output signals, 21 to each Function Block.

Any one of the 68 inputs can be programmed to be connected to any number of the 84 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity.

Routability is not an issue in that any UIM input can drive any UIM output or multiple outputs without additional delay.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion at the input pin, Macrocell outputs and Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function. This offers an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such Macrocell outputs programmed onto the same UIM output thus emulate a 3-state bus line. If one of the Macrocell outputs is enabled, the UIM output assumes that same level.

Outputs

Thirty-four of the 36 Macrocell drive chip outputs directly through individually programmable inverters followed by 3-state output buffers; each can be individually controlled by the Output Enable product term mentioned above. An additional configuration option disables the output permanently. One dedicated FastOE input can also be configured to control any of the chip outputs instead of, or in conjunction with the individual OE product term.

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip flop. Latch and flip-flop can be programmed with either of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they

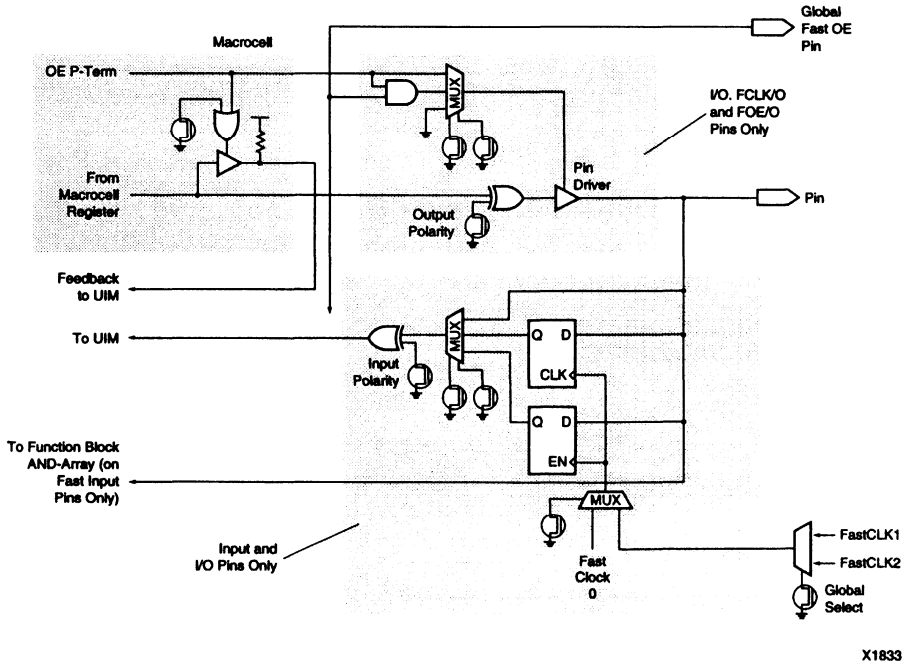


Figure 3. Input/Output Schematic

incur the combinatorial delay in the device, provided the one-clock-period pipeline latency is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

3.3 V or 5 V Interface configuration

The XC7236/A can be used in systems with two different supply voltages, 5 V or 3.3 V. The device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O output drivers (V_{CCIO}). V_{CCINT} is always connected to a nominal +5 V supply, but V_{CCIO} may be connected to either +5 V or +3.3 V, depending on the output interface requirement.

When V_{CCIO} is connected to +5 V, the input thresholds are TTL levels, and thus compatible with 5 V or 3.3 V logic, and the output high levels are compatible with 5 V systems. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7236/A ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed such that the I/O can also safely interface to a mixed 3.3-V or 5-V bus.

FastDecode and FastCompare

The FastDecode unit contains four fast programmable 6-bit decoders with a common set of six inputs (FDI). Each decoder compares the data on the inputs against a pre-programmed 6-bit fixed value and drives a designated chip output (FDO). Each decoder is programmable with Don't Care bits, and each can indicate match either active High or Low as a programmable option.

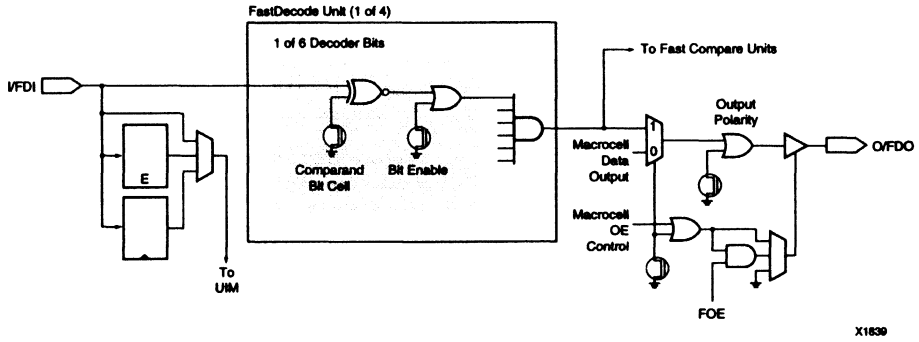


Figure 4a. FastDecode Schematic

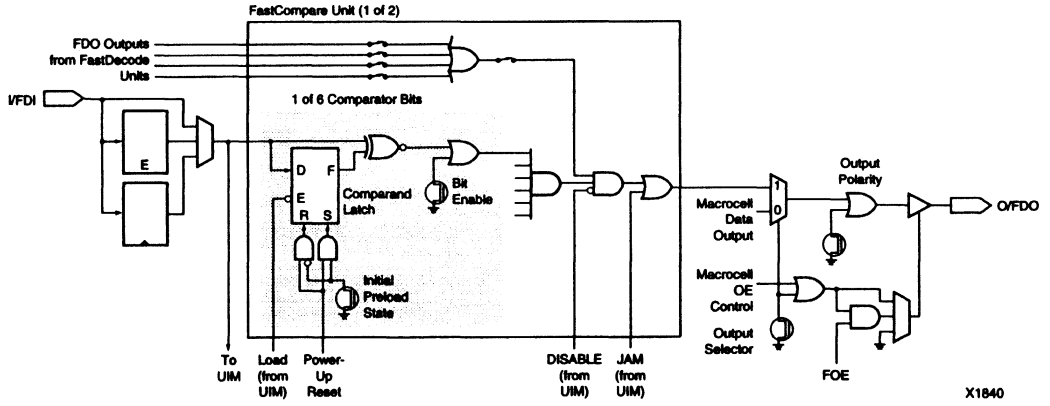


Figure 4b. FastCompare Schematic

The FastCompare unit contains two fast programmable 6-bit comparators with a common set of six inputs (FCI), separate from the FDI inputs . Each comparator compares the data on the inputs against a pattern stored in its six latches and drives a designated chip output (FCO). Data can be loaded into these latches either from the FastCompare data inputs, or can be preloaded during chip configuration (Power-up or Reset). Each comparator is programmable with Don't Care bits and can be conditioned with the result of one or more of the FastDecode FDO outputs.

The comparison can be disabled (forced false) and the polarity of the match response can be chosen.

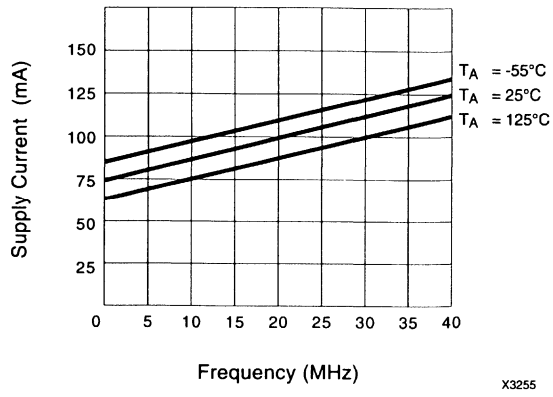
Since this compare circuitry bypasses the UIM and Macrocells, it is very fast and can also be used as high-speed address decoder.

Programming and Using the XC7236/A

The features and capabilities described above are used by the Xilinx development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex format. Programming support is available from a number of programmer manufacturers. The UIM connections and Function Block AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among EPLD devices, requires either a very fast



Typical Power Requirements for XC7236/A Configured as Eight 4-bit Counters (V_{CC} = +5.0 V, V_{IN} = 0 or 5 V, all outputs open)

V_{CC} rise time (<5 µs) or the application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. The latter can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the Macrocell registers.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to 7.0	V
V_{TS}	Voltage applied to 3-state output	–0.5 to 7.0	V
T_{STG}	Storage temperature	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter			Min	Max	Units
V_{CCINT}	Supply voltage relative to GND	Commercial	t_A = 0°C to 70°C	4.75	5.25	V
V_{CCIO}	Supply voltage relative to GND	Industrial	t_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	t_C = –55°C to 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage 3.3 V			3.0	3.6	V
V_{IL}	Low-level input voltage			0	0.8	V
V_{IH}	High-level input voltage			2.0	V_{CC}+ 0.3	V
V_O	Output voltage			0	V_{CCIO}	V

DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL high-level output voltage	I/O = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V high-level output	I/O = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V low-level output voltage	I/O = 12 mA V_{CC} = Min		0.5	V
	3.3 V low-level output voltage	I/O = 10 mA V_{CC} = Min		0.4	V
I_{CC}	Supply Current	V_{IN} = 0 V V_{CC} = Max f = 0 MHz		100	µA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10	µA
I_{OZ}	Output High-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10	µA
C_{IN}	Input capacitance (sample tested)	V_{IN} = GND f = 1.0 MHz		10	pF

AC Timing Requirements

			XC7236				XC7236A				
	Speed Grade		-30		-25		-20		-16 (Com/Ind Only)		
Description	**Fig.**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Sequential toggle frequency (with feedback) using FastCLK	5	f_{CYC} (Note 1)	0	33	0	40	0	50	0	60	MHz
Sequential toggle frequency (with feedback) using a Product-Term clock	5	f_{CYC1} (Note 1)	0	33	0	40	0	50	0	60	MHz
Macrocell toggle frequency using local feedback and FastCLK		f_{CYC4} (Note 5)	0	42	0	50	0	50	0	60	MHz
Macrocell register transmission frequency (without feedback) using FastCLK		f_{CLK} (Note 5)	0	36	0	45	0	50	0	60	MHz
Macrocell register transmission frequency (without feedback) using a Product-Term clock		f_{CLK1} (Note 5)	0	36	0	42	0	50	0	60	MHz
Input register transmission frequency (without feedback) using FastCLK		f_{CLK2} (Note 5)	0	42	0	50	0	50	0	60	MHz
Input register to Macrocell register pipeline freq. using FastCLK	6	f_{CLK3} (Note 1)	0	25	0	33	0	40	0	60	MHz
FastCLK Pulse width (High/Low)	10	t_W	12		10		8		6		ns
Product-Term clock pulse width (active/inactive)	10	t_{W1}	14		12		9		7		ns
Input to Macrocell register set-up time before FastCLK	8	t_{SU}	35		29		24		18		ns
Input to Macrocell register hold time after FastCLK	8	t_H	-7		-7		-4		-4		ns
Input to Macrocell register set-up time before Product-Term clock	7	t_{SU1} (Note 1)	19		16		14		10		ns
Input to Macrocell register hold time after Product-Term clock	7	t_{H1}	0		0		0		0		ns
Input register/latch set-up time before FastCLK	9	t_{SU2}	10		8		8		6		ns
Input register/latch hold time after FastCLK	9	t_{H2}	0		0		0		0		ns
FastCompare input set-up time before latch-enable input	11	t_{SU3}	4		2		2		2		ns
FastCompare input hold time after latch-enable input	11	t_{H3}	18		14		14		12		ns
FastCompare input hold time after comparator jam asserted	11	t_{H4}	30		25		25		22		ns
FastInput to Macrocell register set-up time before FastCLK		t_{SU5}	26		20		18		15		ns
FastInput to Macrocell register hold time after FastCLK		t_{H5}	0		0		0		0		ns
Set/reset pulse width (active)	10	t_{WA}	15		12		12		10		ns
Set/reset input recovery set-up time before FastCLK	10	t_{RA}	36		30		25		20		ns

AC Timing Requirements (Continued)

			XC7236				XC7236A				
	Speed Grade		-30		-25		-20		-16 (Com/Ind Only)		
Description	Fig.	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Set/reset input hold time after FastCLK	10	t_{HA}	-5		-5		0		0		ns
Set/reset input recovery time before P-Term clock	10	t_{RA1}	18		15		15		12		ns
Set/reset input hold time after P-Term clock	10	t_{HA1}	12		9		9		8		ns
Set/reset input hold time after reset/set inactive		t_{HRS}	12		10		10		8		ns
FastCompare latch-enable pulse width	10	t_{WC}	22		16		16		12		ns

Propagation Delays

			XC7236				XC7236A				
	Speed Grade		-30		-25		-20		-16 (Com/Ind Only)		
Description	Fig.	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
FastCLK input to registered output delay	10	t_{CO}	5	17	5	14	3	13	3	10	ns
P-Term clock input to registered output delay	10	t_{CO1}	10	36	10	30	5	24	5	20	ns
Set/reset input to registered output delay	10	t_{AO}	10	48	10	40	5	32	5	25	ns
Input to nonregistered output delay	10	t_{PD} (Note 1)	10	48	10	40	5	32	5	25	ns
FastCompare or FastDecode input to FastCompare output	11	t_{PDC}	5	26	5	23	3	23	3	20	ns
FastCompare DISABLE or JAM input to FastCompare output	11	t_{PDC1}	5	30	5	25	3	24	3	22	ns
FastDecode data input to FastDecode output delay		t_{PDC3}	5	18	5	15	3	15	3	14	ns
Input to output enable	10	t_{OE}	10	37	10	32	5	25	5	20	ns
Input to output disable	10	t_{OD}	10	37	10	32	5	25	5	20	ns
FastInput to non-registered Macrocell output delay		t_{PD5}	10	39	10	31	5	25	5	20	ns
FastInput to output enabled		t_{OE5}	5	28	5	23	3	20	3	15	ns
FastInput to output disabled		t_{OD5}	5	28	5	23	3	20	3	15	ns
FOE input to output enabled		t_{FOE}	5	18	5	15	3	14	3	12	ns
FOE input to output disabled		t_{FOD}	5	18	5	15	3	14	3	12	ns

Notes: 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

Incremental Parameters

			XC7236				XC7236A				
Speed Grade			**-30**		**-25**		**-20**		**-16** (Com/Ind Only)		
Description	**Fig**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Arithmetic carry delay between adjacent Macrocells	12	t_{PDT1} (Note 2)		1.5		1.2		1.2		1	ns
Arithmetic carry delay through 9 adjacent Macrocells in a Function Block	12	t_{PDT8} (Note 2)		8		6		5		3	ns
Arithmetic carry delay through 10 Macrocells from Macrocell #n to Macrocell #n in next F Block	12	t_{PDT9} (Note 2)		12		9		6		4	ns
Incremental delay from UIM-input (for P-Term clock) to registered Macrocell feedback	13	t_{COF1}		14		12		7		5	ns
Incremental delay from FastCLK net to latched/registered UIM-input	13	t_{COF2} (Note 3)		1		1		1		1	ns
Incremental delay from UIM-input to nonregistered Macrocell feedback	13	t_{PDF} (Note 1)		26		22		14		10	ns
Incremental delay from UIM-input (set/reset) to registered Macrocell feedback	13	t_{AOF}		26		22		14		10	ns
Incremental delay from UIM-input (used as output-enable/disable) to Macrocell feedback	13	t_{OEF}, t_{ODF}		15		14		7		5	ns
Propagation delay through unregistered Input pad (to UIM) plus output pad driver (from Macrocell)	13	t_{IN} + t_{OUT} (Note 4)		22		18		18		15	ns

Power-up/Reset Timing Parameters

Description	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Master Reset input Low pulse width	t_{WMR}	100			ns
V_{CC} rise time (if MR not used for power-up)	t_{rVCC} (Note 6)			5	µs
Configuration completion time (to outputs operational)	t_{RESET}		350	1000	µs

Notes:
1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for an adder with registered outputs.
3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-Macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).
4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a Macrocell output (feedback point) to an output or I/O pin. Only the sum of t_{IN} + t_{OUT} can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.
5. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.
6. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset and Set inputs must not be asserted until all applicable input and feedback set-up times are met.

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and Macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 5 defines the max clock frequency (with feedback). Any Macrocell output can be fed back to the UIM as an input for the next clock cycle. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 6 specifies the max operating frequency (f_{CLK3})for pipelined operation between the input registers and the Macrocell registers, using FastCLK.

Figure 7 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 8 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 9 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 10 shows the waveforms for the Macrocell and control paths.

Figure 11 defines the FastCompare timing parameters.

Figure 12 defines the carry propagation delays between Macrocells and between Function Blocks. The parameters describe the delay from the CIN, D1 and D2 inputs of a Macrocell ALU to the CIN input of the adjacent Macrocell ALU. These delays must be added to the standard Macrocell delay path (t_{PD} or t_{SU})to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard Macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

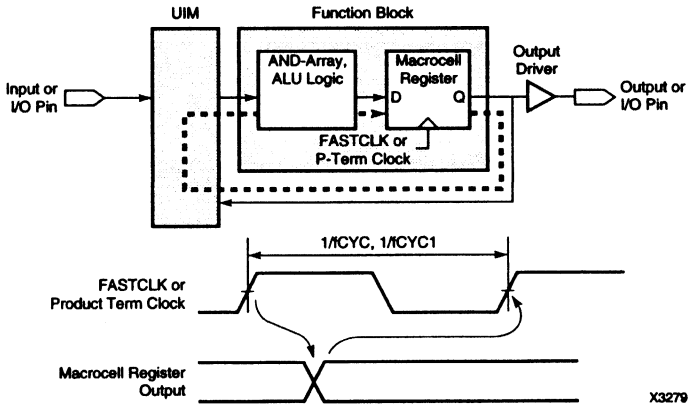


Figure 5. Delay Path Specifications for f_{CYC} and f_{CYC1}

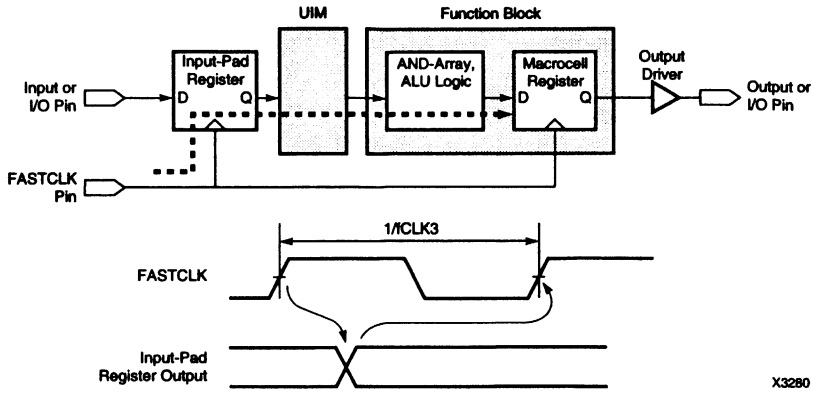


Figure 6. Delay Path Specification for f_{CLK3}

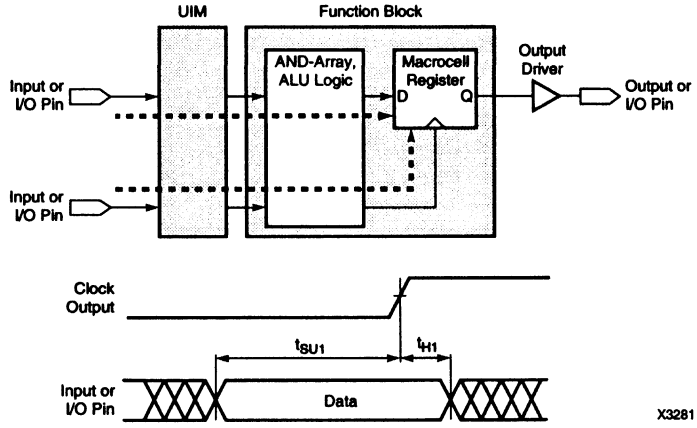


Figure 7. Delay Path Specification for t_{SU1} and t_{H1}

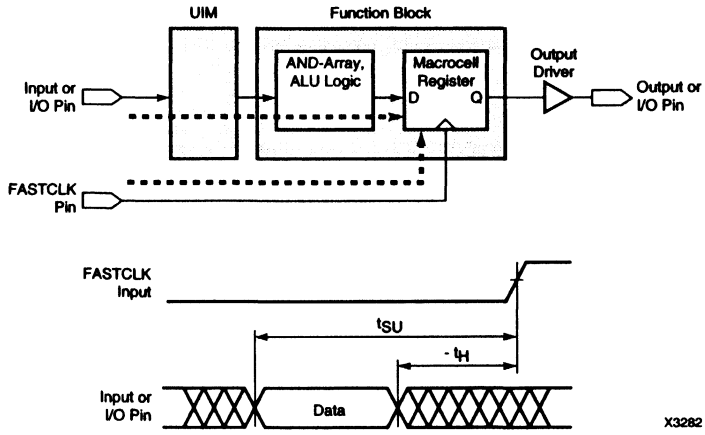


Figure 8. Delay Path Specification for t_{SU} and t_H

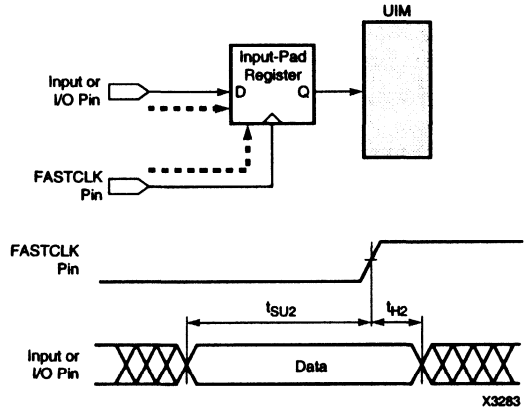


Figure 9. Delay Path Specification for t_{SU2} and t_{H2}

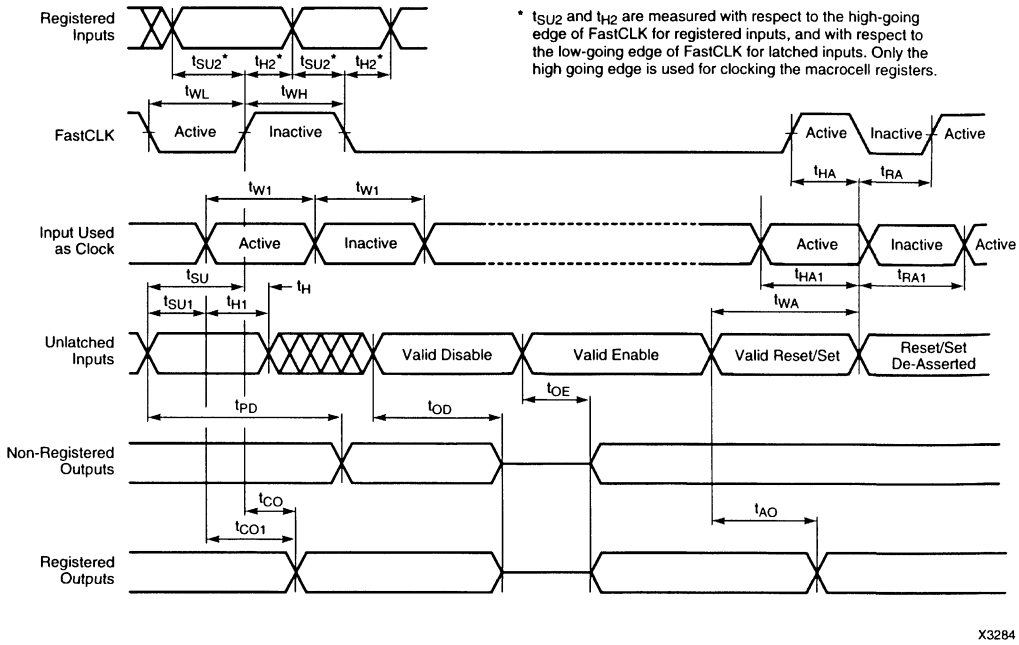


Figure 10. Principal Pin-to-Pin Measurements

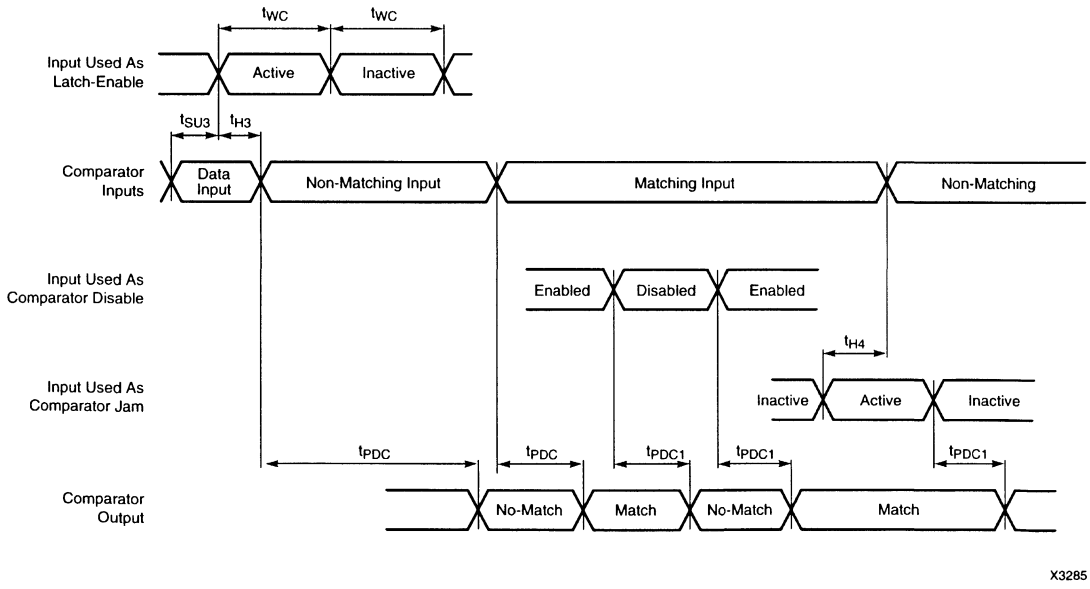


Figure 11. FastCompare Timing Waveforms

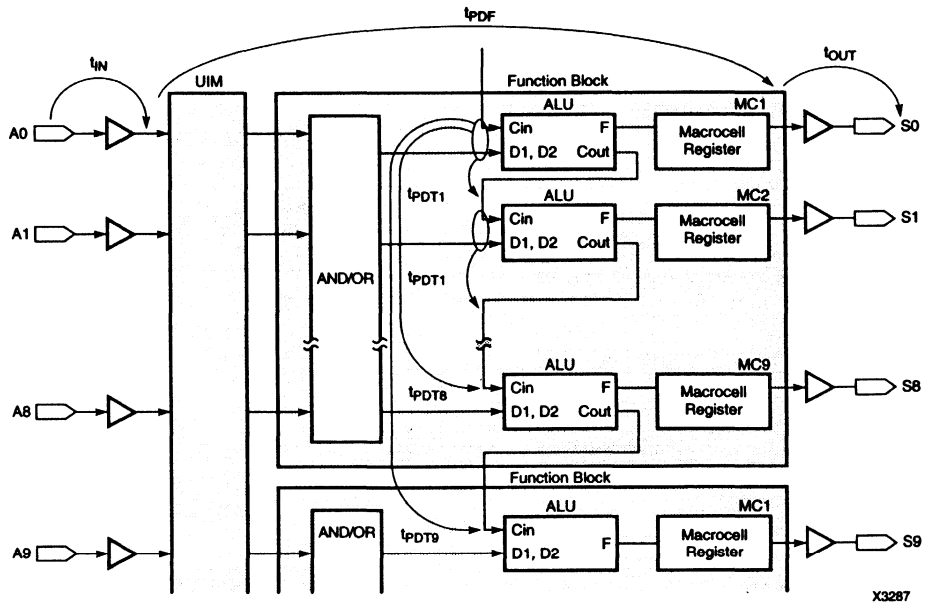


Figure 12. Arithmetic Timing Parameters

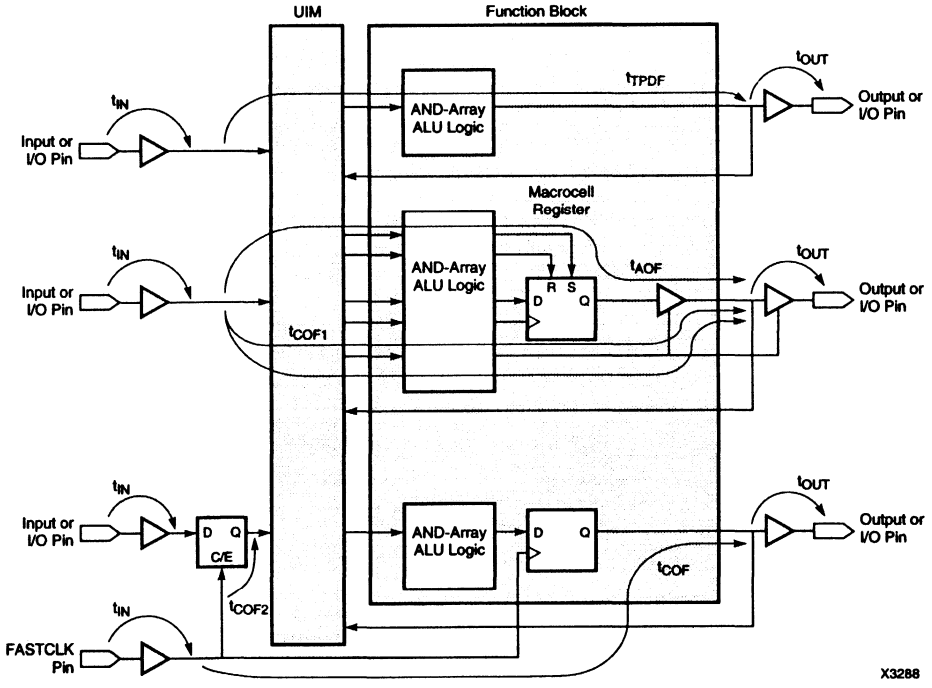


Figure 13. Incremental Timing Parameters

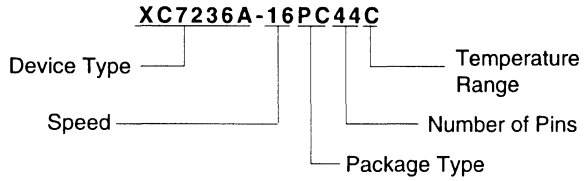
44-Pin LCC Pinouts

Pin #	Input	Output
1	Master Reset V_{PP}	
2	Input/FCI	MC2-1
3	Input/FCI	
4	Input/FCI	
5	Input/FCI	MC2-4
6	Input/FCI	MC2-5
7	GND	
8	Input/FCI	MC2-6
9	FastCLK0	MC2-7
10	FastCLK1	MC2-8
11	FastCLK2	MC2-9
12	V_{CCIO}	
13	Input	MC1-1
14	Input	MC1-2
15	Input	MC1-3
16	Input	MC1-4
17	GND	
18	Input	MC1-5
19	Input	MC1-6
20	Input/FI	MC1-7
21	Input/FI	MC1-8
22	Input/FI	MC1-9

Pin #	Input	Output
23	V_{CCIO}	
24	Input/FI	MC4-9/FCO
25	Input/FI	MC4-8/FCO
26	Input/FI	MC4-7
27	Input	MC4-6
28	Input	MC4-5
29	GND	
30	Input	MC4-4
31	Input	MC4-3
32	FastOE	MC4-2
33	Input	MC4-1/FDO
34	V_{CCINT}	
35	Input/FI	MC3-9/FDO
36	Input/FI	MC3-8/FDO
37	Input/FI	MC3-7/FDO
38	Input/FDI	MC3-6
39	GND	
40	Input/FDI	MC3-5
41	Input/FDI	MC3-4
42	Input/FDI	MC3-3
43	Input/FDI	MC3-2
44	Input/FDI	MC3-1

FI = Fast Input FCI = FastCompare input FDI = FastDecode input FCO = FastCompare output FDO = FastDecode output

Ordering Information



Device Options

XC7236
XC7236A

Speed Options

XC7236
-30 30 ns (33 MHz) sequential cycle time
-25 25 ns (40 MHz) sequential cycle time

XC7236A
-25 25 ns (40 MHz) sequential cycle time
-20 20 ns (50 MHz) sequential cycle time
-16 16 ns (60 MHz) sequential cycle time (commercial and industrial only)

Package Options

PC44 44-Pin Plastic Leaded Chip Carrier
WC44 44-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C to 125°C (Case)

XC7272A
72 Macrocell CMOS EPLD

Preliminary Product Specifications

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 72 Macrocells, grouped into eight Function Blocks, interconnected by a programmable Universal Interconnect Matrix
- Each Function Block contains a programmable AND-array with 21 complementary inputs, providing up to 16 product terms per Macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each Macrocell
  - Dedicated fast carry network between Macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all Macrocell logic paths
- 72 signal pins in the 84-pin packages
  - 42 I/Os, 12 inputs, 18 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O-pin is usable as input when Macrocell is buried
- Two high-speed, low-skew global clock inputs
- 68-pin and 84-pin leaded chip carrier packages and 84-pin Pin-Grid-Array packages

General Description

The XC7272A is a second-generation High Density Programmable Logic Device that combines the classical features of the PAL-like EPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output Macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each Macrocell. Dedicated fast arithmetic carry lines running directly between adjacent Macrocells and Function Blocks support fast adders, subtractors and comparators of any length up to 72 bits.

This additional ALU in each Macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent Macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and Macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Functional Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 72 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7272A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Automated design mapping is supported by Xilinx development software based on design capture using third-party schematic entry tools, PLD compilers or direct text-based equation files. Design mapping is completed in a few minutes on a PC.

Architectural Overview

Figure 1 shows the XC7272A structure. Eight Function Blocks (FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output Macrocells that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macrocells drive a 3-state chip output, all feed back into the UIM.

The device also contains two dedicated Fast Comparators (FCs) for address compare or decode functions. The following pages describe the elements of this architecture in detail.

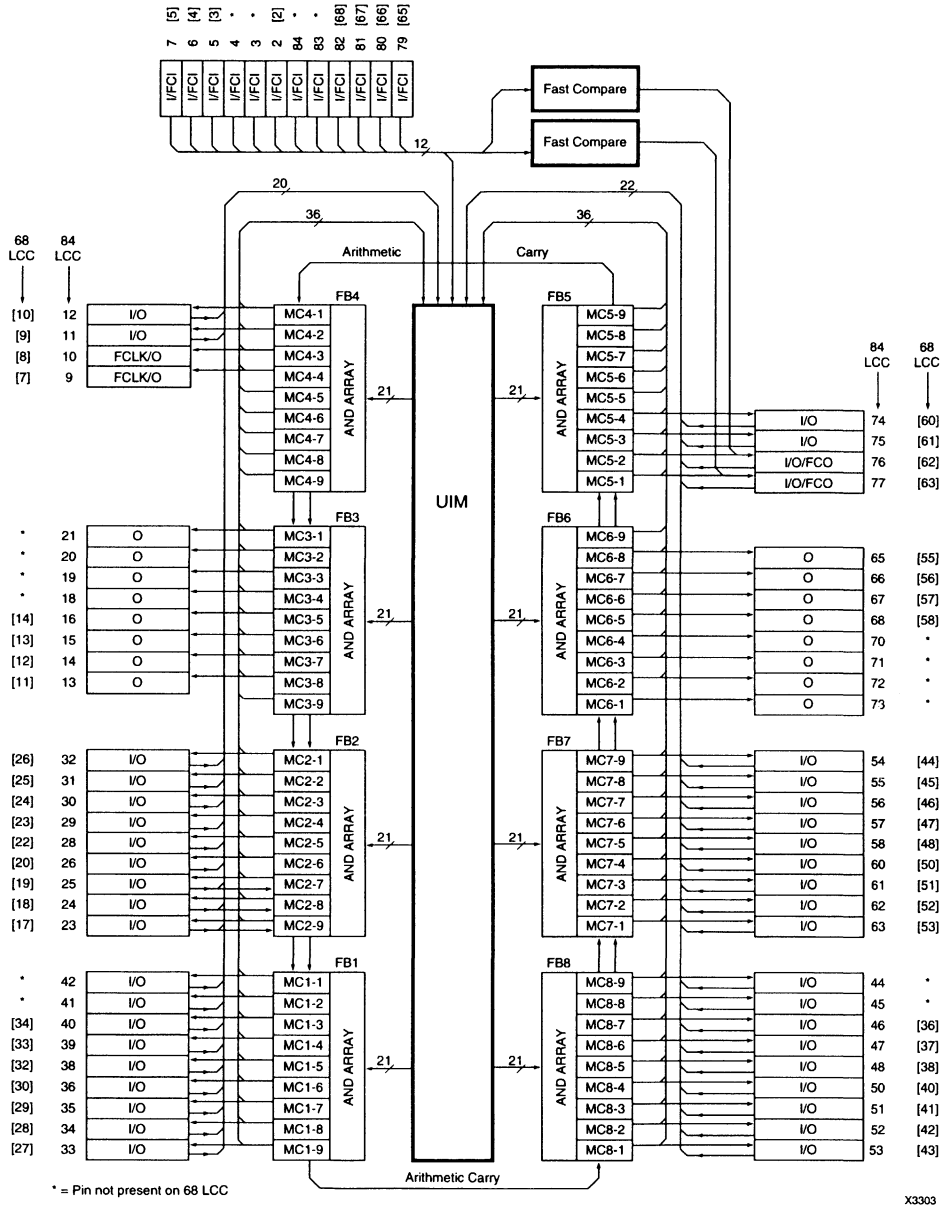


Figure 1. XC7272A Architecture

Function Blocks and Macrocells

The XC7272A contains 72 Macrocells with identical structure, grouped into eight Function Blocks of nine Macrocells each. Each Macrocell is driven by product terms derived from the 21 inputs from the UIM into the Function Block.

Five product terms are private to each Macrocell; an additional 12 product terms are shared among the nine Macrocells in any Function Block. One of the private product terms is a dedicated clock for the flip-flop in the Macrocell. See the description on page 3-24 for other clocking options.

The remaining four private product terms can be selectively ORed together with up to three of the shared product terms, and drive one input to an Arithmetic Logic Unit. The other input to the ALU is driven by the OR of up-to-nine product terms from the remaining shared product terms.

As a programmable option, two of the private product terms can be used for other purposes. One is the asynchronous active-High Reset of the Macrocell flip-flop, the other can be either an asynchronous active-High Set of the Macrocell flip-flop, or an Output-Enable signal.

The Arithmetic Logic Unit has two programmable modes: In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to max 16 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the lower Macrocell; it also feeds a carry output to the next higher Macrocell. This carry propagation chain crosses the boundaries between Function Blocks, but it can also be configured 0 or 1 when it enters a Function Block.

This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture, when trying to perform arithmetic functions like add, subtract, and magnitude compare.

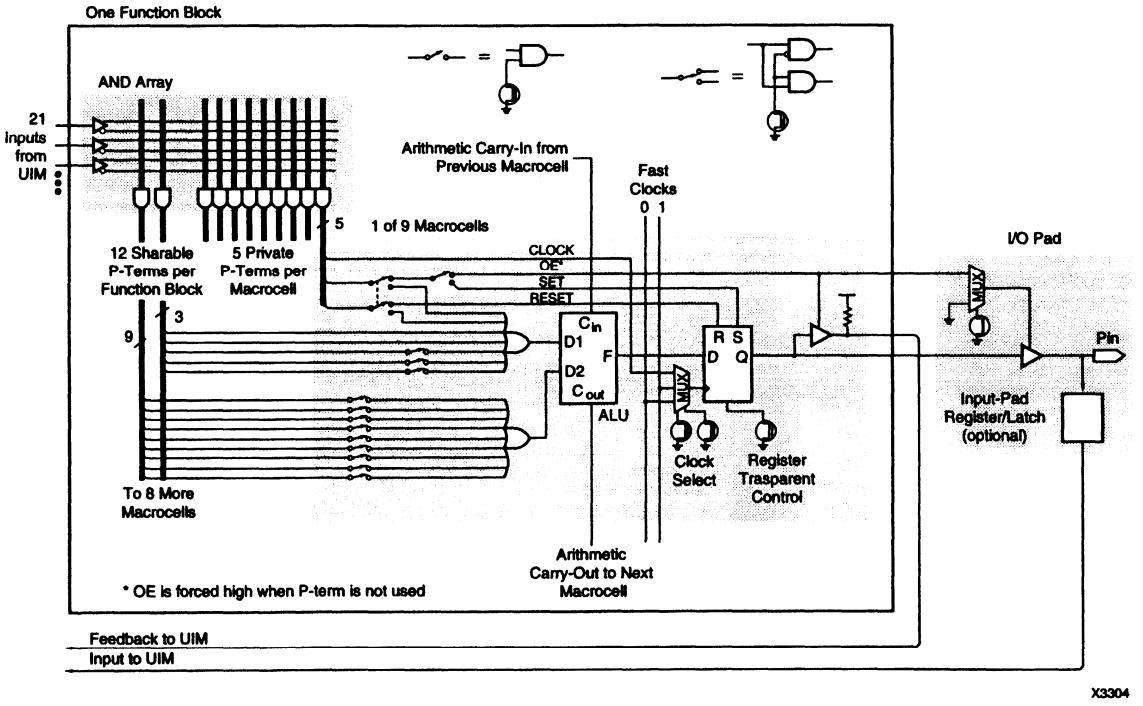


Figure 2. Function Block and Macrocell Schematic Diagram

The ALU output drives the D input of the Macrocell flip-flop.

Each flip-flop has several programmable options:

One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock.

If this option is *not* programmed, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable: It is either the dedicated product term mentioned above, or it is one of the two global FastCLK signals that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each Macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving the chip output buffer, the Macrocell output is also routed back as an input to the UIM. When the Output Enable product term mentioned above is not active, this feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 126 inputs: 72 from the 72 Macrocells, 42 from bidirectional I/O pins, and 12 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 168 output signals, 21 to each Function Block.

Any one of the 126 inputs can be programmed to be connected to any number of the 168 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity. Routability is not an issue: Any UIM input can drive any UIM output, even multiple outputs, and the delay is constant.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion in the Macrocell outputs and the Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function, thus offering an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such Macrocell outputs programmed onto the same UIM output thus emulate a 3-state bus line. If one of

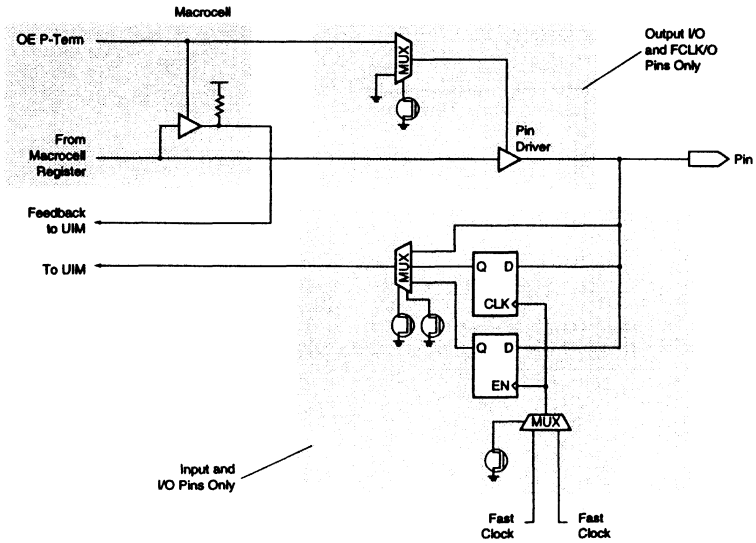


Figure 3. Input/Output Schematic Diagram

the Macrocell outputs is enabled, the UIM output assumes that same level.

Outputs

Sixty of the 72 Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. For bidirectional I/O pins, an additional programmable cell can optionally disable the output permanently. The buried flip-flop is then still available for internal feedback, and the pin can still be used as a separate input

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip-flop. Latch and flip-flop can be programmed with either of the two FastCLK signals as latch enable or clock. The latch is transparent when FastCLK is High, and the flip-flop clocks on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, in cases where a pipeline cycle is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

FastCompare

Two 12-bit wide fast identity (equality) comparators are driven by the 12 dedicated FCI inputs, which also drive into the UIM. These dedicated circuits compare the input data against two sets of 12-bit data, either loaded previously from the same data inputs, or pre-programmed into the device.

As a programming option, any bit can be excluded from the comparison (disabled), the whole comparison can be disabled (forced false), and the polarity of the response can be chosen. The FCO comparator outputs can substitute the MC 5-1 and 5-2 outputs. Since this compare circuitry bypasses the UIM and the AND/OR logic, it is very fast and can also be used as a high-speed address decoder.

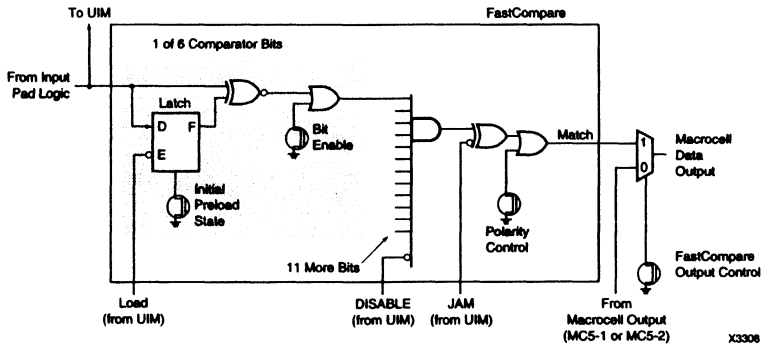


Figure 4. FastCompare Schematic Diagram

Programming and Using the XC7272A

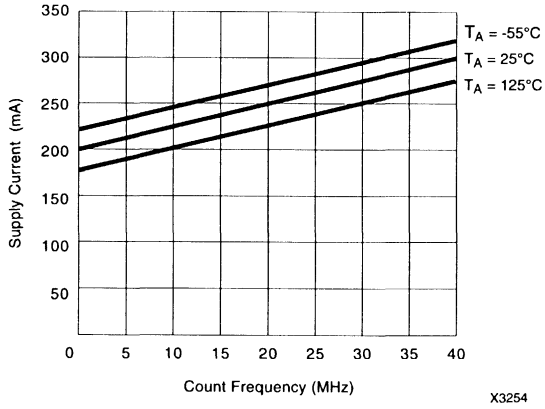
The features and capabilities described above are used by the Xilinx development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex format. Programming support is available from a number of programmer manufacturers. The UIM connections and Function Block AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among EPLD devices, requires either a very fast V_{CC} rise time (<5 µs) or the application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. The latter can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the macrocell registers.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input-pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.



Typical Power Requirements for XC7272A Configured as Sixteen 4-bit Counters
(V_{CC} = +5.0 V, V_{IN} = V_{CC} or GND, all outputs open)

Absolute Maximum Ratings

			Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to 7.0	V
V_{TS}	Voltage applied to 3-state output	–0.5 to 7.0	V
T_{STG}	Storage temperature	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

				Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	t_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	t_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	t_C = –55°C to 125°C	4.5	5.5	V
V_{IH}	High-level input voltage			2.0	V_{CC}+ 0.3	V
V_{IL}	Low-level input voltage			0	0.8	V

DC Characteristics Over Operating Conditions

		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4 mA , Vcc min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 8 mA , Vcc min		0.5	V
I_{CC}	Supply current while idle		250	mA
I_{IL}	Input Leakage current	–10	+10	µA
I_{OZ}	Output High-Z leakage current	–100	+100	µA
C_{IN}	Input capacitance (sample tested)		10	pF

AC Timing Requirements

Description	Fig	Symbol	-25 Min	-25 Max	-20 Min	-20 Max	-16 (Com/Ind Only) Min	-16 (Com/Ind Only) Max	Units
Sequential toggle frequency (with feedback) using FastCLK	5	f_{CYC} (Note 1)	0	40	0	50	0	60	MHz
Sequential toggle frequency (with feedback) using a Product-Term clock	5	f_{CYC1} (Note 1)	0	40	0	50	0	60	MHz
Macrocell register transmission frequency (without feedback) using FastCLK		f_{CLK} (Note 5)	0	59	0	60	0	60	MHz
Macrocell register transmission frequency (without feedback) using a Product-Term clock		f_{CLK1} (Note 5)	0	50	0	50	0	60	MHz
Input register transmission frequency (without feedback) using FastCLK		f_{CLK2} (Note 5)	0	67	0	67	0	67	MHz
Input register to Macrocell register pipeline frequency using FastCLK	6	f_{CLK3} (Note 1)	0	40	0	50	0	60	MHz
FastCLK Low pulse width	10	t_{WL}	7.5		7.5		6		ns
FastCLK High pulse width	10	t_{WH}	7.5		7.5		6		ns
Product-Term clock pulse width (active/inactive)	10	t_{W1}	10		9		7		ns
Input to Macrocell register set-up time before FastCLK	8	t_{SU}	24		19		15		ns
Input to Macrocell register hold time after FastCLK	8	t_{H}	-7		-4		-4		ns
Input to Macrocell register set-up time before Product-Term clock	7	t_{SU1} (Note 1)	10		8		6		ns
Input to Macrocell register hold time after Product-Term clock	7	t_{H1}	0		0		0		ns
Input register/latch set-up time before FastCLK	9	t_{SU2}	8		8		6		ns
Input register/latch hold time after FastCLK	9	t_{H2}	0		0		0		ns

AC Timing Requirements (Continued)

		Speed Grade	-25		-20		-16 (Com/Ind Only)		
Description	**Fig.**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
FastCompare input set-up time before latch-enable input	11	t_{SU3}	2		2		2		ns
FastCompare input hold time after latch-enable input	11	t_{H3}	14		12		10		ns
FastCompare input hold time after comparator jam asserted	11	t_{H4}	25		22		18		ns
Set/reset pulse width	10	t_{WA}	12		10		8		ns
Set/reset input recovery set-up time before FastCLK	10	t_{RA}	20		20		16		ns
Set/reset input hold time after FastCLK	10	t_{HA}	-5		-3		-3		ns
Set/reset input recovery time before P-Term clock	10	t_{RA1}	6		5		4		ns
Set/reset input hold time after P-Term clock	10	t_{HA1}	9		8		6		ns
Set/reset input hold time after reset/set inactive		t_{HRS}	10		8		6		ns
FastCompare latch-enable pulse width	10	t_{WC}	16		14		12		ns

Propagation Delays

		Speed Grade	-25		-20		-16 (Com/Ind Only)		
Description	**Fig.**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
FastCLK input to registered output delay	10	t_{CO}	5	16	3	14	3	12	ns
P-Term clock input to registered output delay	10	t_{CO1}	10	30	6	25	6	21	ns
Set/reset input to registered output delay	10	t_{AO}	13	40	8	32	8	25	ns
Input to nonregistered output delay	10	t_{PD} (Note 1)	13	40	8	32	8	25	ns
FastCompare input to MATCH output	11	t_{PDC}	8	23	5	22	5	20	ns
FastCompare disable input to MATCH output	11	t_{PDC1}	8	25	5	22	5	20	ns
FastCompare jam input to MATCH output	11	t_{PDC2}	8	25	5	22	5	20	ns
Input to output enable	10	t_{OE}	11	32	7	25	7	22	ns
Input to output disable	10	t_{OD}	11	32	7	25	7	22	ns

Notes 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

Incremental Parameters

	Speed Grade		-25		-20		-16 (Com/Ind Only)		
Description	**Fig**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Arithmetic carry delay between adjacent Macrocells	12	t_{PDT1} (Note 2)		1.6		1.2		1	ns
Arithmetic carry delay through 9 adjacent Macrocells in a Function Block	12	t_{PDT8} (Note 2)		10		8		6	ns
Arithmetic carry delay through 10 Macrocells from Macrocell #n to Macrocell #n in next F Block	12	t_{PDT9} (Note 2)		14		12		10	ns
Incremental delay from FastCLK net to registered output feedback	13	t_{COF}		1		1		1	ns
Incremental delay from UIM-input (for P-Term clock) to registered Macrocell feedback	13	t_{COF1}		15		12		10	ns
Incremental delay from FastCLK net to latched/registered UIM-input	13	t_{COF2} (Note 3)		1		1		1	ns
Incremental delay from UIM-input to nonregistered Macrocell feedback	13	t_{PDF} (Note 1)		25		19		14	ns
Incremental delay from UIM-input (set/reset) to registered Macrocell feedback	13	t_{AOF}		25		19		14	ns
Incremental delay from UIM-input (used as output-enable/disable) to Macrocell feedback	13	t_{OEF}, t_{ODF}		17		12		11	ns
Propagation delay through unregistered Input pad (to UIM) plus output pad driver (from Macrocell)	13	$t_{IN} + t_{OUT}$ (Note 4)		15		13		11	ns

Power-up/Reset Timing Parameters

Description	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Master Reset input Low pulse width	t_{WMR}	100			ns
V_{CC} rise time (if MR not used for power-up)	t_{rVCC}			5	µs
Configuration completion time (to outputs operational)	t_{RESET}		350	1000	µs

Notes 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for an adder with registered outputs.

3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-Macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).

4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a Macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

5. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and Macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 5 defines the max clock frequency (with feedback). Any Macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 6 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the Macrocell registers, using FastCLK.

Figure 7 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 8 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 9 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 10 shows the waveforms for the Macrocell and control paths.

Figure 11 defines the FastCompare timing parameters.

Figure 12 defines the carry propagation delays between Macrocells and between Function Blocks. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a Macrocell ALU to the C_{IN} input of the adjacent Macrocell ALU. These delays must be added to the standard Macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard Macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

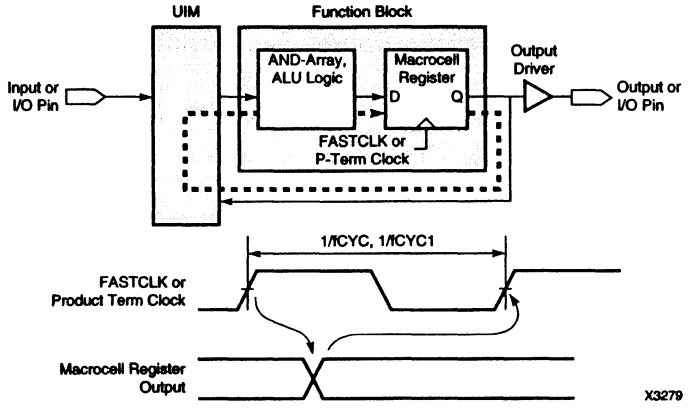


Figure 5. Delay Path Specifications for f_{CYC} and f_{CYC1}

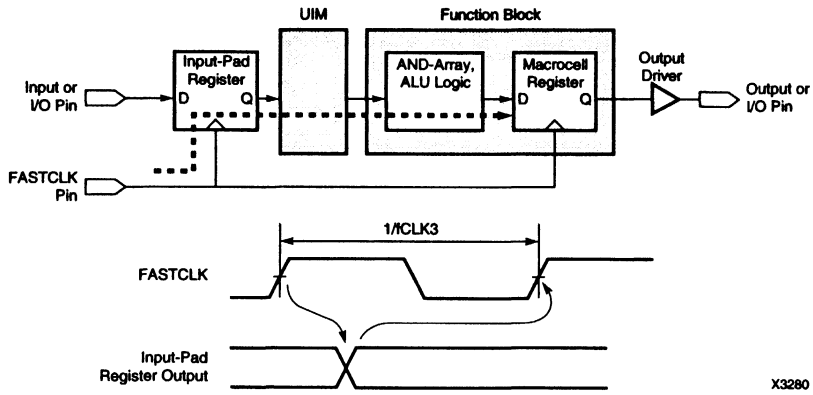


Figure 6. Delay Path Specification for f_{CLK3}

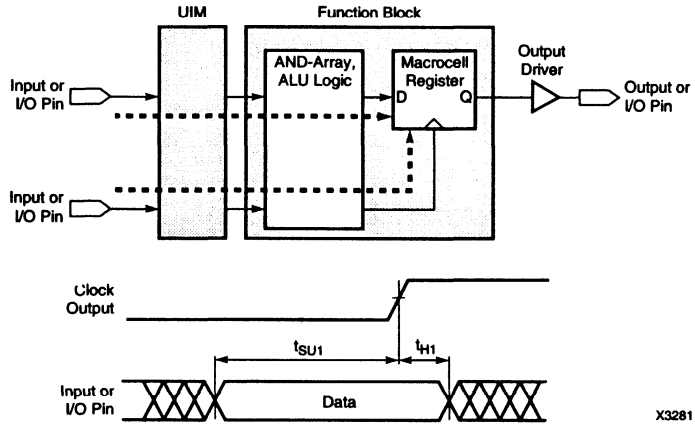


Figure 7. Delay Path Specification for t_{SU1} and t_{H1}

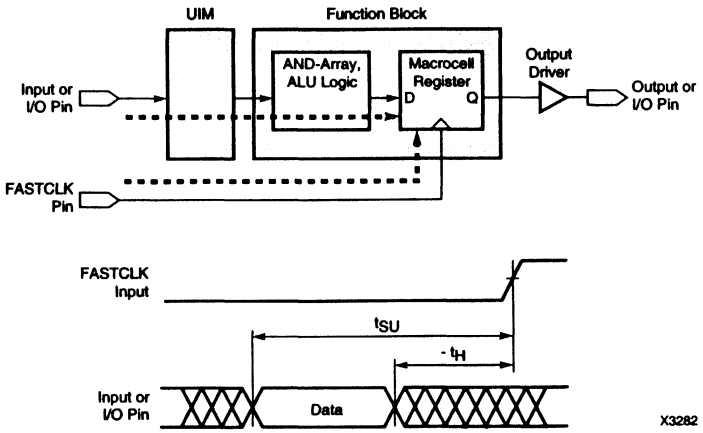


Figure 8. Delay Path Specification for t_{SU} and t_H

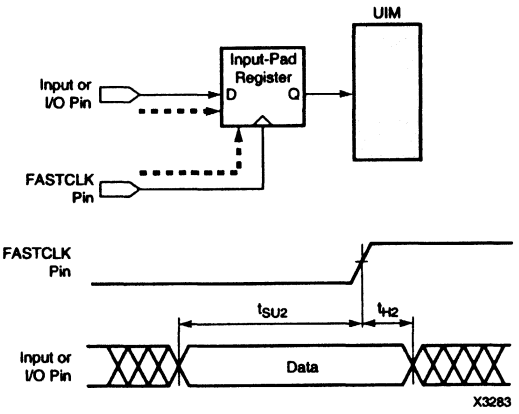


Figure 9. Delay Path Specification for t_{SU1} and t_{H1}

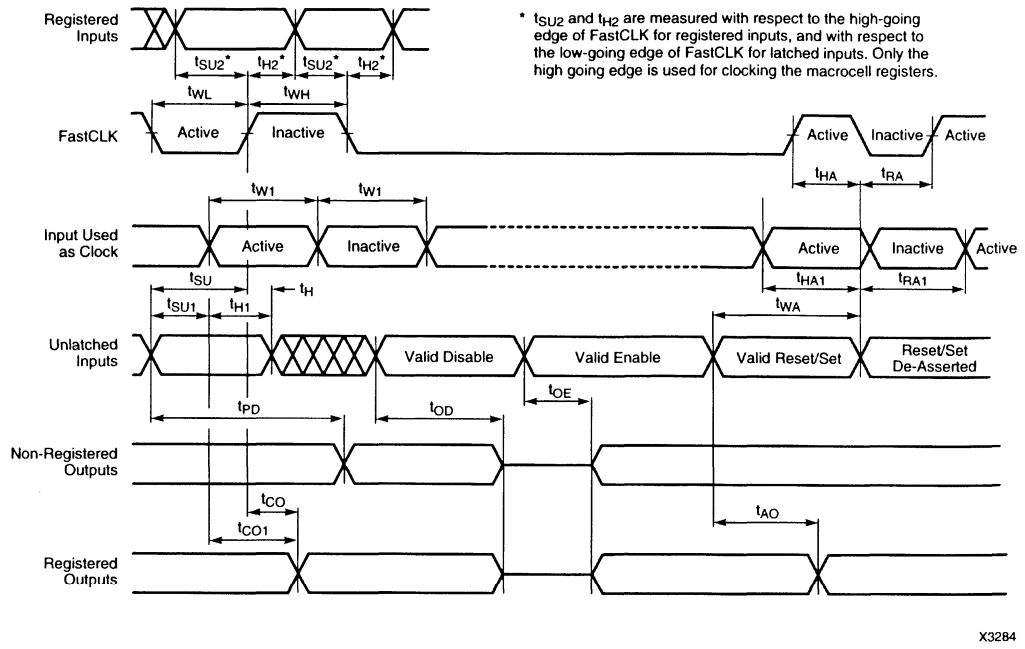


Figure 10. Principal Pin-to-Pin Measurements

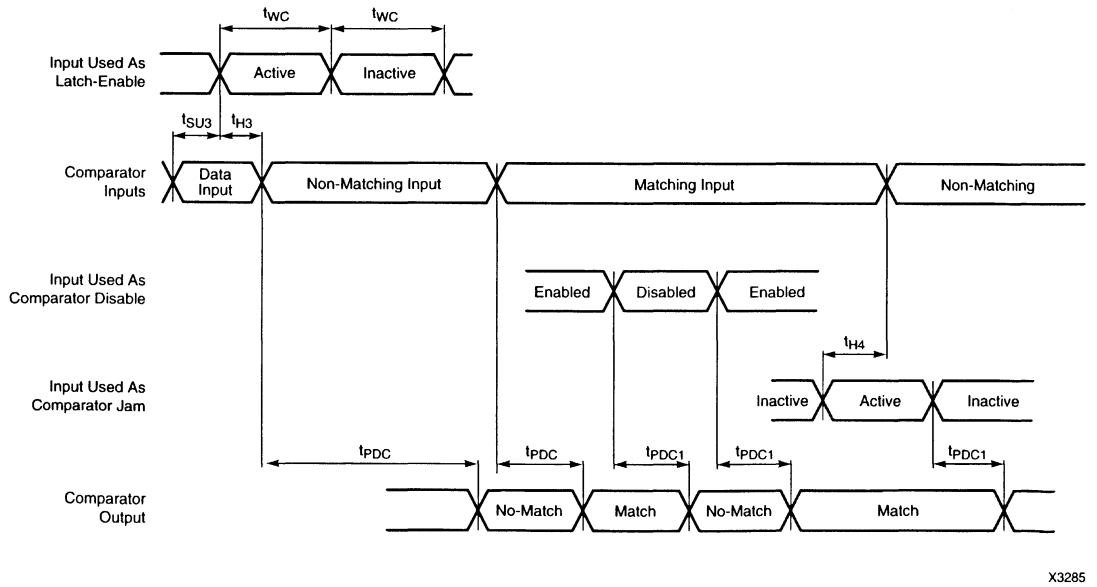


Figure 11. FastCompare Timing Waveforms

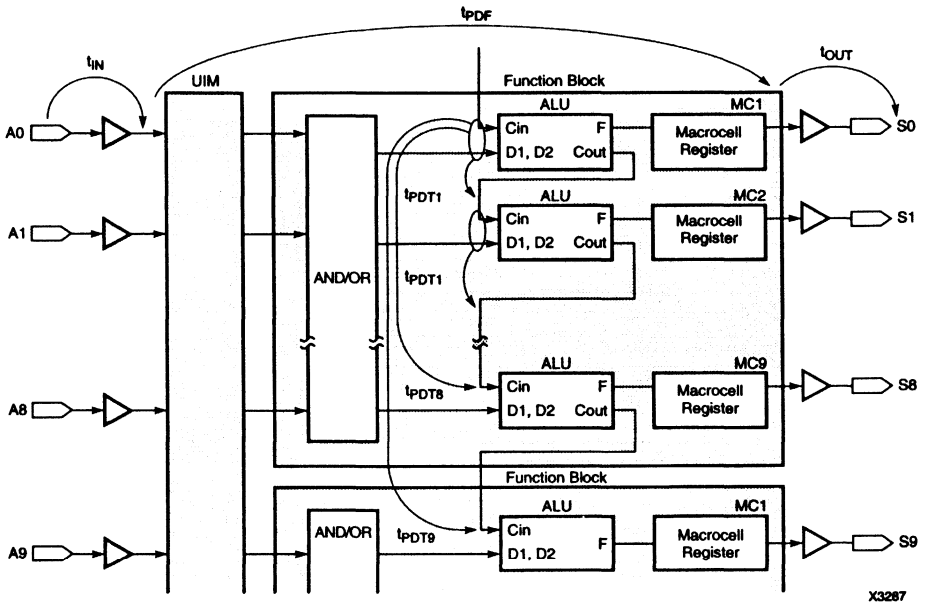


Figure 12. Arithmetic Timing Parameters

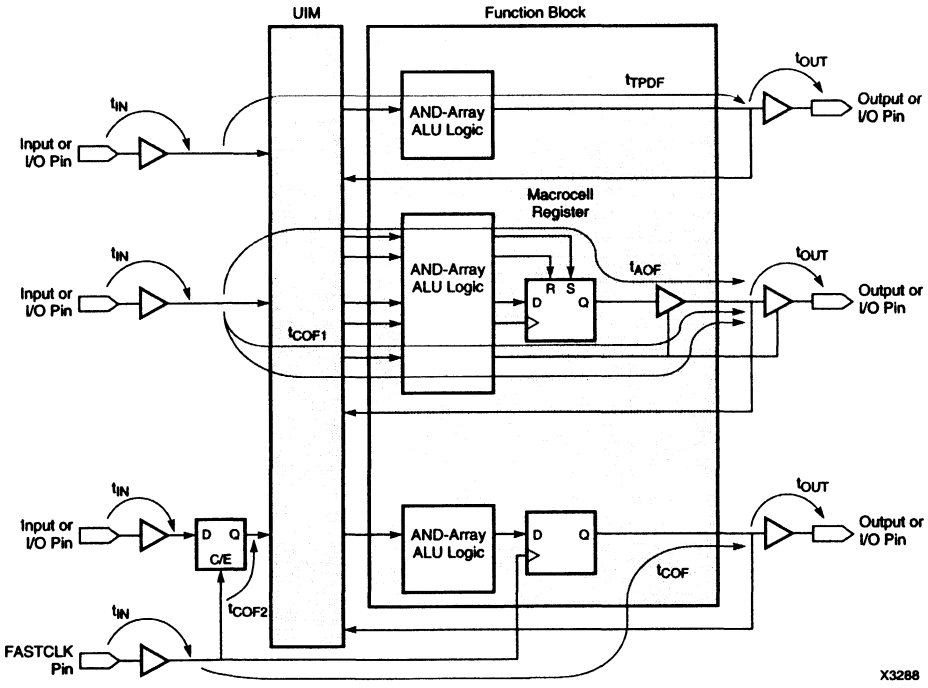


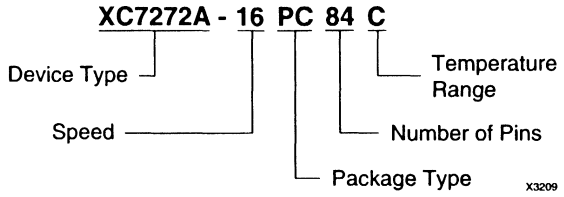
Figure 13. Incremental Timing Parameters

68-Pin LCC, 84-Pin LCC and PGA Pinouts

68 LCC	In	XC7272A	out	84 LCC	84 PGA
1	Master Reset V_{PP}			1	F-9
2	Input/FCI			2	F-11
-	Input/FCI			3	E-11
-	Input/FCI			4	E-10
3	Input/FCI			5	E-9
4	Input/FCI			6	D-11
5	Input/FCI			7	D-10
6	GROUND			8	C-11
7	Fast CLK0		MC4-4	9	B-11
8	Fast CLK1		MC4-3	10	C-10
9	Input		MC4-2	11	A-11
10	Input		MC4-1	12	B-10
11			MC3-8	13	B-9
12			MC3-7	14	A-10
13			MC3-6	15	A-9
14			MC3-5	16	B-8
15	GROUND			17	A-8
-			MC3-4	18	B-6
-			MC3-3	19	B-7
-			MC3-2	20	A-7
-			MC3-1	21	C-7
16	Vcc			22	C-6
17	Input		MC2-9	23	A-6
18	Input		MC2-8	24	A-5
19	Input		MC2-7	25	B-5
20	Input		MC2-6	26	C-5
21	GROUND			27	A-4
22	Input		MC2-5	28	B-4
23	Input		MC2-4	29	A-3
24	Input		MC2-3	30	A-2
25	Input		MC2-2	31	B-3
26	Input		MC2-1	32	A-1
27	Input		MC1-9	33	B-2
28	Input		MC1-8	34	C-2
29	Input		MC1-7	35	B-1
30	Input		MC1-6	36	C-1
31	GROUND			37	D-2
32	Input		MC1-5	38	D-1
33	Input		MC1-4	39	E-3
34	Input		MC1-3	40	E-2
-	Input		MC1-2	41	E-1
-	Input		MC1-1	42	F-2

68 LCC	In	XC7272A	out	84 LCC	84 PGA
35	Vcc			43	F-3
-	Input		MC8-9	44	G-3
-	Input		MC8-8	45	G-1
36	Input		MC8-7	46	G-2
37	Input		MC8-6	47	F-1
38	Input		MC8-5	48	H-1
39	GROUND			49	H-2
40	Input		MC8-4	50	J-1
41	Input		MC8-3	51	K-1
42	Input		MC8-2	52	J-2
43	Input		MC8-1	53	L-1
44	Input		MC7-9	54	K-2
45	Input		MC7-8	55	K-3
46	Input		MC7-7	56	L-2
47	Input		MC7-6	57	L-3
48	Input		MC7-5	58	K-4
49	GROUND			59	L-4
50	Input		MC7-4	60	J-5
51	Input		MC7-3	61	K-5
52	Input		MC7-2	62	L-5
53	Input		MC7-1	63	K-6
54	Vcc			64	J-6
55			MC6-8	65	J-7
56			MC6-7	66	L-7
57			MC6-6	67	K-7
58			MC6-5	68	L-6
59	GROUND			69	L-8
-			MC6-4	70	K-8
-			MC6-3	71	L-9
-			MC6-2	72	L-10
-			MC6-1	73	K-9
60	Input		MC5-4	74	L-11
61	Input		MC5-3	75	K-10
62	Input		MC5-2/FCO	76	J-10
63	Input		MC5-1/FCO	77	K-11
64	GROUND			78	J-11
65	Input/FCI			79	H-10
66	Input/FCI			80	H-11
67	Input/FCI			81	F-10
68	Input/FCI			82	G-10
-	Input/FCI			83	G-11
-	Input/FCI			84	G-9

Ordering Information



Speed Options

-25 25 ns (40 MHz) sequential cycle time
-20 20 ns (50 MHz) sequential cycle time
-16 16 ns (60 MHz) sequential cycle time (commerial and industrial only)

Package Options

PC68 68-Pin Plastic Leaded Chip Carrier
WC68 68-Pin Windowed Ceramic Leaded Chip Carrier
PC84 84-Pin Plastic Leaded Chip Carrier
WC84 84-Pin Windowed Ceramic Leaded Chip Carrier
PG84 84-Pin Ceramic Windowed Pin Grid Array

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C to 125°C (Case)

XILINX®

SECTION 4

XC7300 EPLD Family

XILINX®

XC7300 CMOS EPLD Family

Advance Product Information

Features

- High-performance Erasable Programmable Logic Devices (EPLDs)
  - 7.5 to 12 ns pin-to-pin delays
  - 80 to 125 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - Fast Function Blocks
  - High-Density Function Blocks
- 100% interconnect matrix
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 40 MHz 16-bit accumulators
- Multiple independent clocks
- Each input programmable as direct, latched, or registered
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- Supported by industry standard design and verification tools
- Advanced 0.8µ CMOS EPROM process

Description

The XC7300 family employs a unique Dual-Block architecture, which provides high speed operations via Fast Function Blocks and/or high density capability via High Density Function Blocks.

Fast Function Blocks (FFBs) provide fast, pin-to-pin speed and logic throughput for critical decoding and ultra-fast state machine applications. High-density Function Blocks (FBs) provide maximum logic density and system-level features to implement complex functions with predictable timing for adders and accumulators, wide functions and state machines requiring large numbers of product terms, and other forms of complex logic.

In addition, the XC7300 architecture employs the Universal Interconnect Matrix (UIM) which guarantees 100% interconnect of all internal functions. This interconnect scheme provides constant, short interconnect delays for all routing paths through the UIM. Constant interconnect delays simplify device timing and guarantee design performance, regardless of logic placement within the chip.

All XC7300 devices are designed in 0.8µ CMOS EPROM technology.

All XC7300 EPLDs include programmable power management features to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to

The XC7300 Family

	XC7336	XC7354	XC7372	XC73108	XC73144
Typical 22V10 Equivalent	4	6	8	12	16
Number of Macrocells	36	54	72	108	144
Number of Function Blocks	4	6	8	12	16
Number of Flip-Flops	36	108	126	198	234
Number of Fast Inputs	18	24	30	42	54
Number of Signal Pins	48	66	84	120	156

minimize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software supports XC7300 EPLD design using third-party schematic entry tools, HDL compilers, or direct equation-based text files. Using a PC or a workstation and one of these design capture methods, designs are automatically mapped to an XC7300 EPLD in a matter of minutes.

The XC7300 devices are available in plastic and ceramic leaded chip carriers, pin-grid-array (PGA), and quad flat pack (QFP) packages. Package options include both windowed ceramic for design prototypes and one-time programmable plastic versions for cost-effective production volume.

Architecture

The XC7300 architecture consists of multiple programmable Function Blocks interconnected by a UIM as shown in Figure 1. The Dual-Block architecture contains two types of function blocks: Fast Function Blocks and High-Density Function Blocks. Both types of function blocks, and the I/O blocks, are interconnected through the UIM.

Fast Function Blocks

The Fast Function Block receives 24 signals and their complements from the UIM. The 24 inputs can be individually selected from the UIM, 12 fast input pins, or the nine Macrocell feedbacks from the Fast Function Block. The programmable AND array in each Fast Function Block generates 45 product terms to drive the nine Macrocells in each Fast Function Block. Each Macrocell can be configured for registered or combinatorial logic. See Figure 2.

Five product terms from the programmable AND array are allocated to each Macrocell. Four of these product terms are ORed together and drive the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High Set Input to the Macrocell flip-flop. The flip-flop can be configured as transparent for combinatorial outputs.

The programmable clock source is one of two global FastCLK signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

The Fast Function Block Macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individual controlled by one of two dedicated Fast Output Enable inputs, enabled permanently or disabled permanently. The Macrocell output is also routed back as an input to the Fast Function Block, and as an input to the UIM.

Product Term Assignment

The XC7300 family uses a product term assignment scheme that provides product-term flexibility without disabling Macrocell outputs.

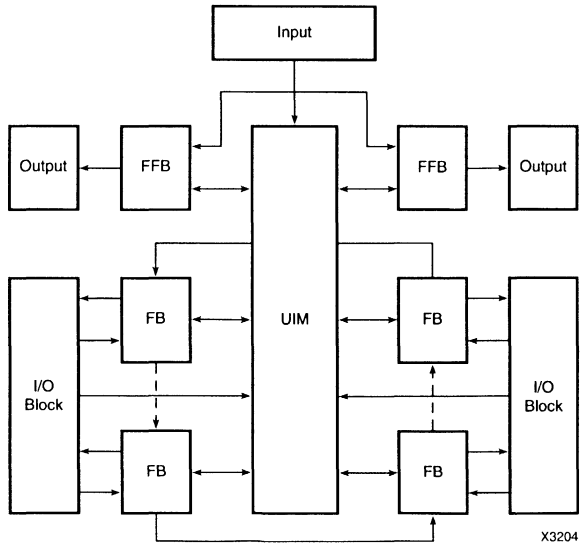


Figure 1. XC7300 Device Block Diagram

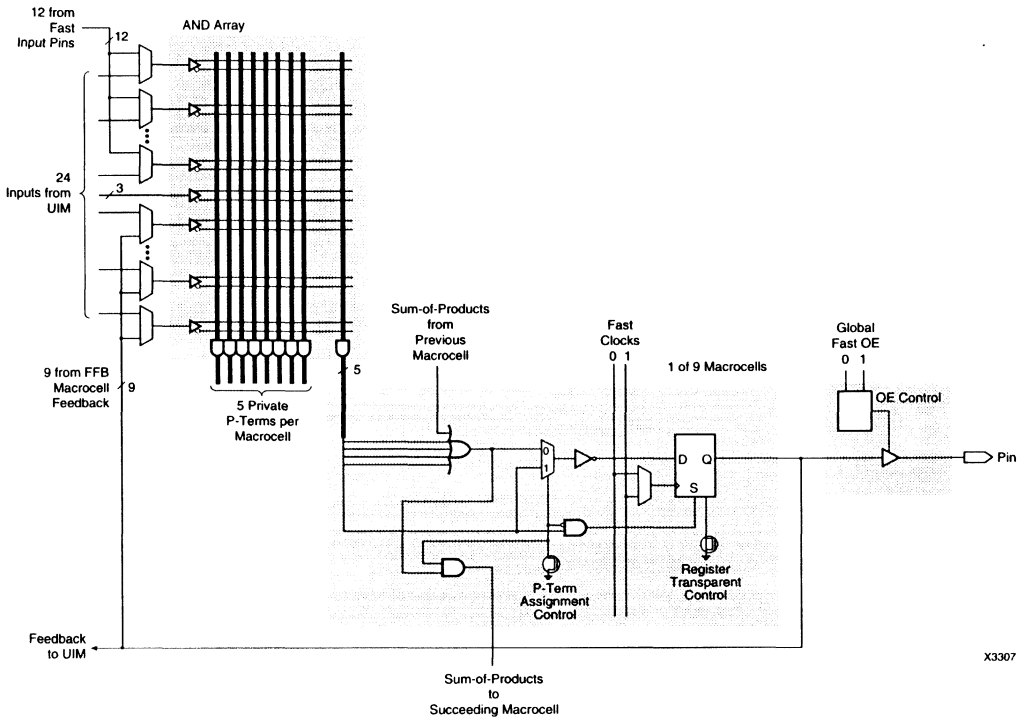


Figure 2. Fast Function Block Macrocell Schematic

The sum-of-product OR gates for each Macrocell can be expanded using the Fast Function Block product term assignment scheme. The product term assignment transfers product terms in increments of four product terms from one Macrocell to the next. Complex logic functions requiring up to 36 product terms can be implemented using product term assignment. When product terms are assigned to adjacent Macrocells, the product term normally dedicated to the Set function becomes the D-input to the Macrocell register. Thus, the Macrocell is still usable while product terms are transferred to adjacent Macrocells (Figure 3).

High-Density Function Blocks

Each member of the XC7300 family contains multiple, High-Density Function Blocks linked though the UIM. Each Function Block contains nine Macrocells. Each Macrocell can be configured for either registered or combinatorial logic. A detailed block diagram of the XC7300 FB is shown in Figure 4.

Each FB receives 21 signals and their complements from the UIM and an additional three inputs from the Fast Input (FI) pins.

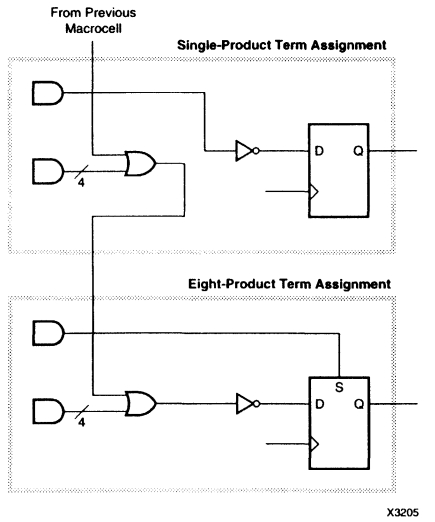


Figure 3. Fast Function Block Product Term Assignment

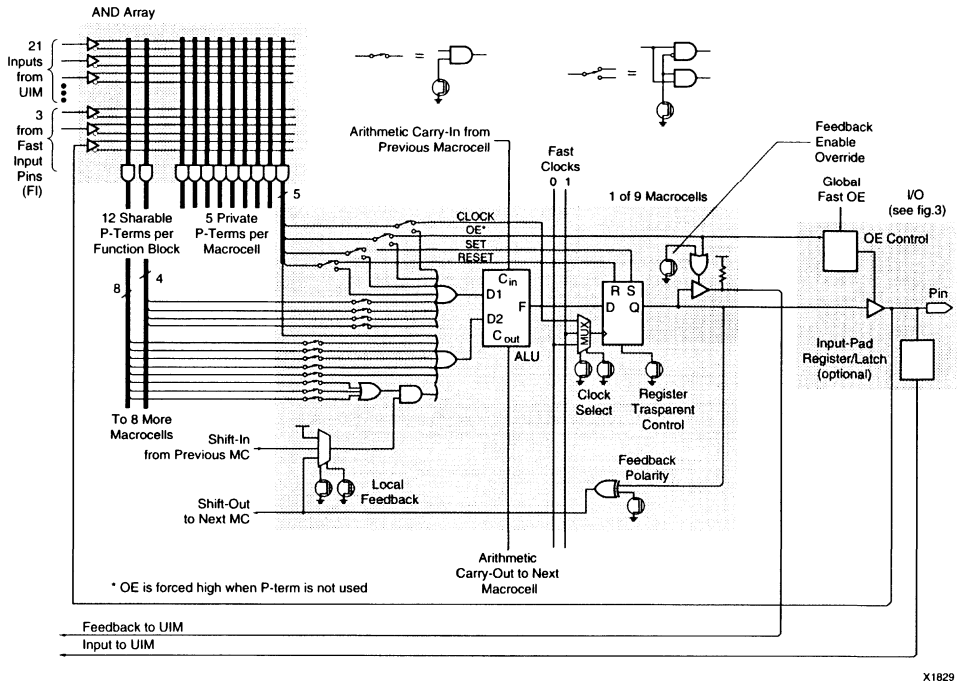


Figure 4. High-Density Function Block and Macrocell Schematic

Shared and Private Product Terms

Each Macrocell contains five private product terms that can be used as the primary inputs for combinatorial functions implemented in the Arithmetic Logic Unit (ALU), or as individual Reset, Set, Output-Enable, and Clock logic functions for the flip-flop. Each Function Block also provides an additional 12 shared product terms, which are uncommitted product terms available for any of the nine Macrocells within the Function Block.

Four private product terms can be ORed together with up to four shared product terms to drive the D1 input to the ALU. The D2 input is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms. The shared product terms add no logic delay, and each shared product term can be connected to one or all nine Macrocells in the Function Block.

Arithmetic Logic Unit

The functional versatility of each Macrocell is enhanced through additional gating and control functions available in the ALU. A detailed block diagram of the XC7300 ALU is shown in Figure 5.

The ALU has two programmable modes; *logic* and *arithmetic*. In logic mode, the ALU functions as a 2-input function generator using a 4-bit look-up table that can be programmed to generate any Boolean function of its D1 and D2 inputs as illustrated in Table I.

The function generator can OR its inputs, widening the OR function to a maximum of 17 inputs. It can AND them, which means that one sum-of-products can be used to mask the other. It can also XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored.

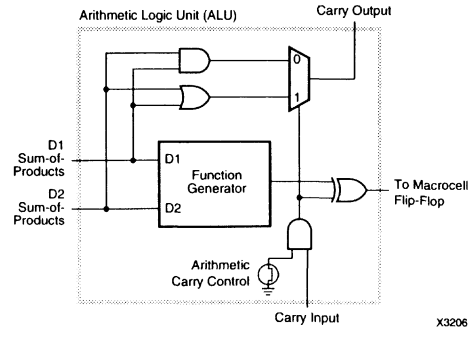


Figure 5. ALU Schematic

Table 1. Function Generator Logic Operations

Function	
D1 :+: D2	$\overline{D1}$:+: $\overline{D2}$
D1 * D2	$\overline{D1}$ * D2
D1 + D2	$\overline{D1}$ + $\overline{D2}$
D1	D2
$\overline{D1}$	$\overline{D2}$
D1 * $\overline{D2}$	$\overline{D1}$ * D2
D1 + $\overline{D2}$	$\overline{D1}$ + D2

Therefore, the ALU can implement one additional layer of logic without any speed penalty.

In arithmetic mode, the ALU block can be programmed to generate the arithmetic sum or difference of the D1 and D2 inputs. Combined with the carry input from the next lower Macrocell, the ALU operates as a 1-bit full adder generating a carry output to the next higher Macrocell. The carry chain propagates between adjacent Macrocells and also crosses the boundaries between Function Blocks. This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture when trying to perform arithmetic functions.

Carry Lookahead

Each Function Block provides a carry lookahead generator capable of anticipating the carry across all nine Macrocells. The carry lookahead generator reduces the ripple-carry delay of wide arithmetic functions such as add, subtract, and magnitude compare to that of the first nine bits, plus the carry lookahead delay of the higher-order Function Blocks.

Macrocell Flip-Flop

The ALU block output drives the input of a programmable D-type flip-flop. The flip-flop is triggered by the rising edge of the clock input, but it can be configured as transparent, making the Q output identical to the D input, independent of the clock, or as a conventional flip-flop.

The Macrocell clock source is programmable and can be one of the private product terms or one of two global FastCLK signals (FCLK0 and FCLK1). Global FastCLK signals are distributed to every Macrocell flip-flop with short delay and minimal skew.

The asynchronous Set and Reset product terms override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set.

In addition to driving the chip output buffer, the Macrocell output is routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output buffer and/or the feedback to the UIM. If it is configured to control UIM feedback, the Output Enable product term forces the UIM feedback line High when the Macrocell output is disabled.

Universal Interconnect Matrix

The UIM receives inputs from Macrocell feedback lines, bidirectional I/O pins, and dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 21 output signals to each High-Density Function Block and 24 output signals to each Fast Function Block.

Any UIM input can be programmed to connect to any UIM output. The delay through the interconnect matrix is constant, regardless of the routing distance and complexity, fan-out, or fan-in. Furthermore, any UIM input can drive one or more UIM outputs with the delay being constant.

When multiple inputs are programmed to be connected to the same output, this output produces the logical AND of the input signals. By choosing the appropriate signal inversions at the input pins, Macrocell outputs and Function Block AND-array input, this AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Programming several such Macrocell outputs onto the same UIM output thus emulates a 3-state bus line. If one of the Macrocell outputs is enabled, the UIM output assumes its level.

Input/Output Blocks

Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. The Macrocell output can be inverted. An additional configuration option allows the output to be disabled permanently. Two dedicated FastOE inputs can also be configured to control any of the chip outputs instead of, or in conjunction with, the individual Output Enable product term. See Figure 6.

Each signal input to the chip is connected to a programmable input structure that can be configured as direct, latched, or registered. The latch and flip-flop can use one of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. The flip-flop includes an active-low clock enable, which when High, holds the present state of the flip-flop and inhibits response to the input signal. The clock enable source is one of two global Clock Enable signals ($\overline{CE0}$ and $\overline{CE1}$). An additional configuration option is polarity inversion for each input signal.

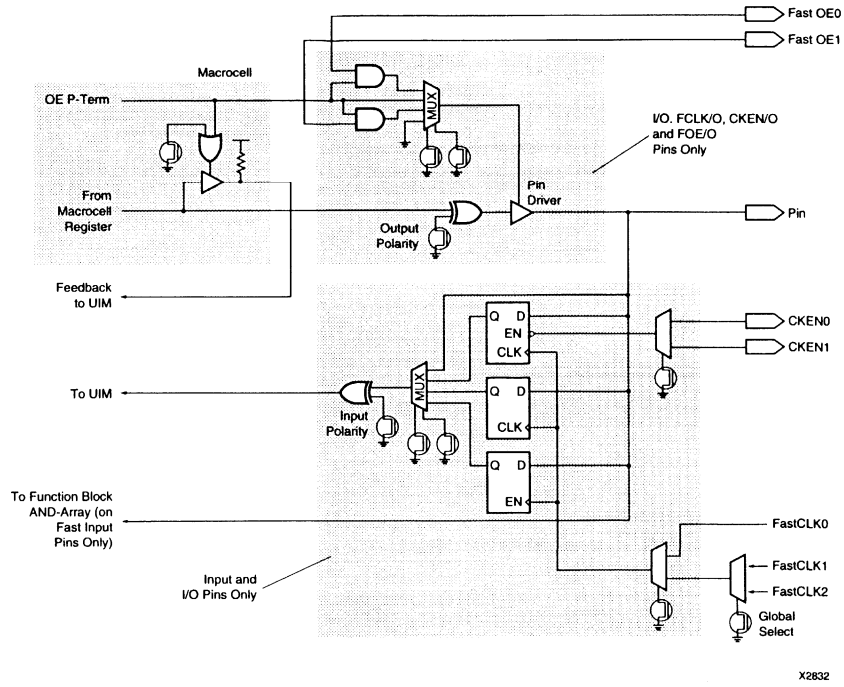


Figure 6. Input/Output Schematic Diagram

3.3 V or 5 V Interface Configuration

XC7300 devices can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7300 device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O drivers (V_{CCIO}). V_{CCINT} must always be connected to a nominal 5 V supply, but V_{CCIO} may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When V_{CCIO} is connected to 5 V, the input thresholds are TTL levels, and thus compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7300 ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so that the I/O can also safely interface to a mixed 3.3 V and 5 V bus.

Power-On Characteristics

Like many highly-flexible EPLDs, the XC7300 devices undergo a short internal initialization sequence upon device powerup. During this time, the outputs remain 3-stated while the device is configured from its internal EPROM array pattern and all registers are initialized. Except for the short delay during device initialization, this operation is completely transparent to the user and typically lasts 200 µs and not more than 300 µs.

For additional flexibility, an active-Low Master Reset pin is provided so that EPLD can be reinitialized even after power is applied. It allows the EPLD to be initialized along with other devices in the system. When it is switched Low, all outputs become 3-stated and the initialization sequence is started. When it returns to High, the outputs become enabled and the device is ready for operation. If this flexibility is not needed, simply connect the Master Reset pin to the device V_{CCINT}.

During the initialization sequence, all input registers or latches are preloaded High, and by default, all FB Macrocell registers are preloaded Low. The FB Macrocell register preload state can be selected by the user. Note that since the device inputs may be active for part of the initialization, key inputs such as Clock, Reset, or Set should remain inactive during initialization to ensure the preloaded registers maintain the correct state before operation.

Power Management

As EPLDs become more complex and system clock frequencies rise, control of on-chip power dissipation becomes increasingly important. The XC7300 power-

management scheme permits non-speed-critical parts of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a small part is speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To further conserve power, unused Macrocells are automatically turned off.

Figure 7 shows typical power requirements for XC73108 device, assuming all Macrocells are enabled and switching at the indicated clock frequency. The two curves shown are for the two extreme cases; all Macrocells in high-performance mode, and all Macrocells in low-power mode. Actual chip dissipation will be between the two curves. The power for each member of the XC7300 family can be calculated for specific operating conditions by using parameters supplied in the individual data sheets.

Erasure Characteristics

In windowed packages, the content of the EPROM array can be erased by exposure to ultraviolet light of wavelengths of approximately 4000 Å. The recommended erasure time is approximately 1 hr. when the device is placed within 1 in. of an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. To prevent unintentional exposure, place opaque labels over the device window.

When the device is exposed to high intensity UV light for much longer periods, permanent damage can occur. The maximum integrated dose the XC7300 EPLD can be exposed to without damage is 7000 W • s/cm^2, or approximately one week at 12,000 $\mu W/cm^2$.å

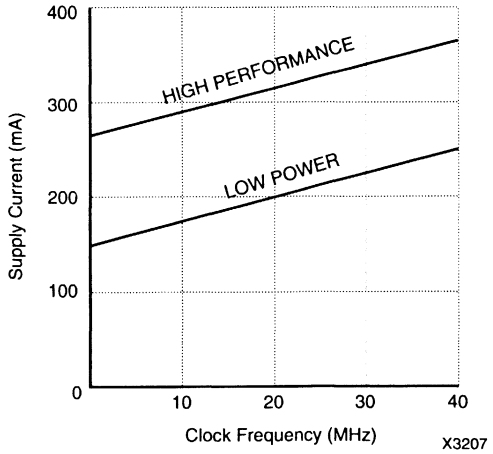


Figure 7. Typical Power Requiements for XC83108

Design Recommendations

For proper operation, all unused input and I/O pins must be connected to a valid logic level (High or Low). The recommended decoupling for all V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Use electrostatic discharge (ESD) handling procedures with the XC7300-series EPLDs to prevent damage to the device during programming, assembly, and test.

Design Security

Each member of the XC7300 family has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fused-based devices. Programmed data within EPROM cells is invisible–even when examined under a microscope–and cannot be selectively erased. The EPROM security bits, and the device configuration data, reset when the device is erased.

High-Volume Production Programming

The XC7300 family offers flexibility for low-volume prototypes as well as cost-effectiveness for high-volume production. The designer can start with ceramic window package parts for prototypes, ramp up initial production using low-cost plastic parts programmed in-house, and then shift into high-volume production using Xilinx factory programmed and tested devices.

The Xilinx factory programmed concept offers significant advantages over competitive masked PLDs, or ASIC redesigns:

- No redesign is required – Even though masked devices are advertised as timing compatible, subtle differences in a chip layout can mean system failure.
- Devices are factory tested – Factory-programmed devices are tested as part of the manufacturing flow, insuring high-quality products.
- Shipments are delivered fast – Production shipments can begin within a few weeks, eliminating masking delays and qualification requirements.

For factory programming procedures, contact your local Xilinx representative.

Timing Model

Timing within the XC7300 EPLDs is easily determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 8.

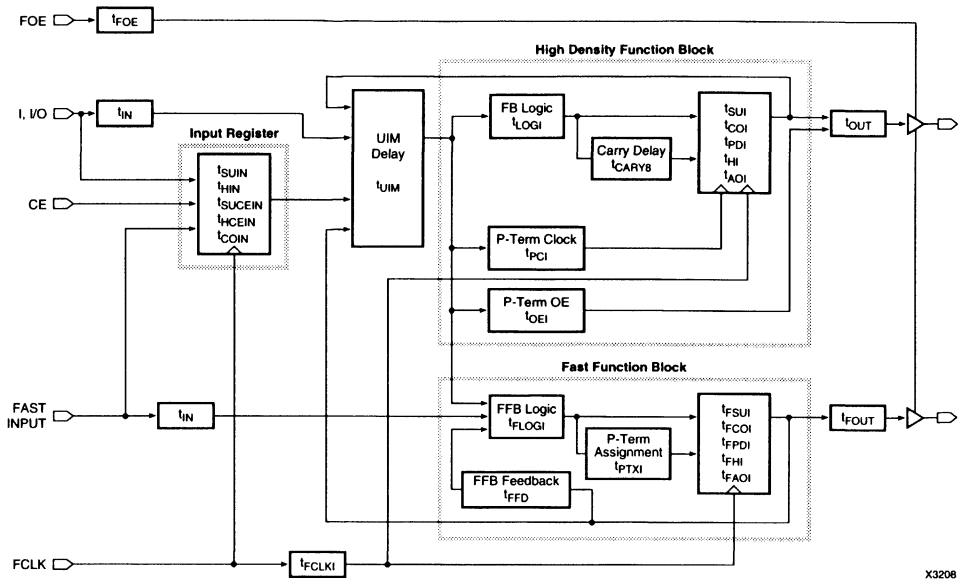


Figure 8. XC7300 Timing Model

The timing model is based on the fixed internal delays of the XC7300 architecture which consists of four basic parts: I/O Blocks, the UIM, Fast Function Blocks and High-Density Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for a particular EPLD.

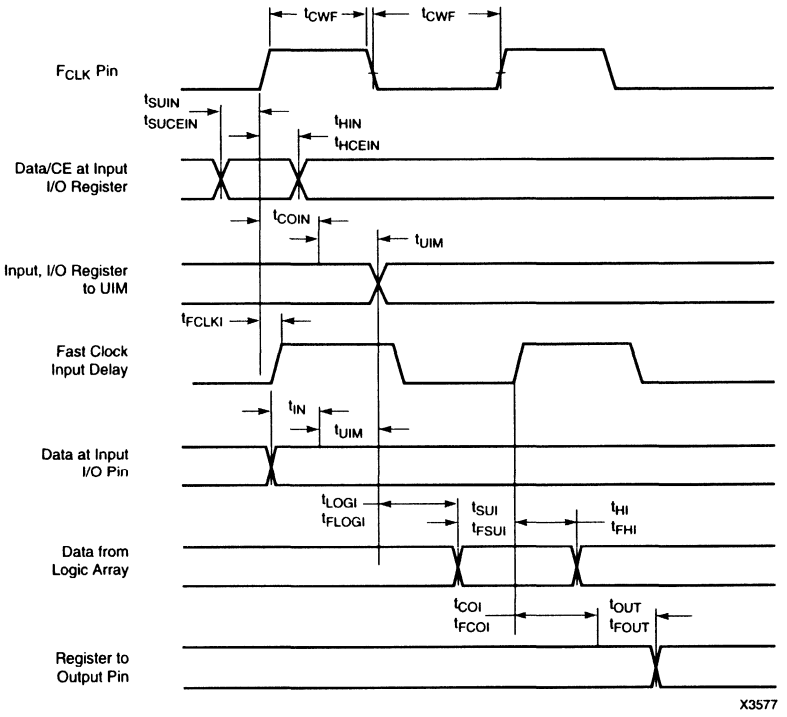
XEPLD Development System

The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator maps the design quickly and automatically onto a chosen EPLD device, produces documentation for design analysis and creates a programming file to configure the device.

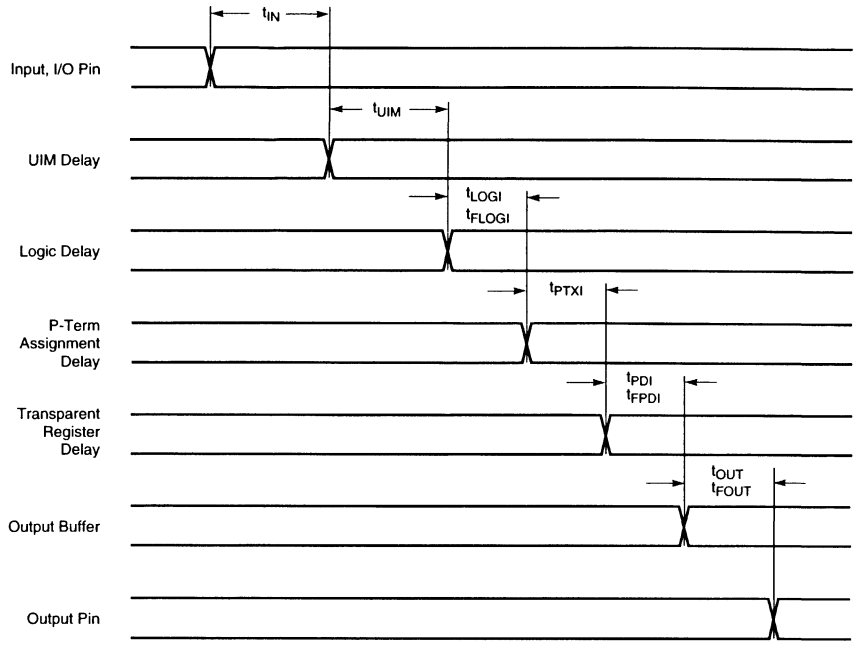
The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques
- Converts netlist to fuse map in minutes using a '486 PC or workstation platform
- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages
- Schematic library with familiar and powerful TTL-like components, including PLDs and ALUs
- Predictable timing even before design entry, using library components and Boolean equations
- Timing simulation using Viewsim, OrCAD VST, and other tools controlled by the Xilinx Design Manager (XDM) program

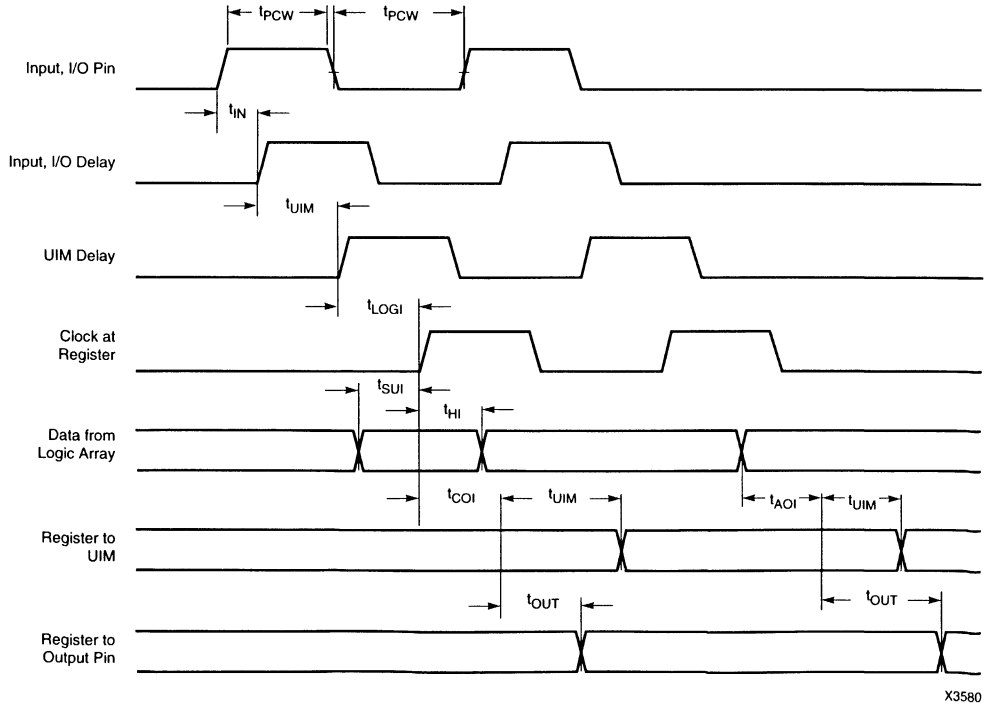
Synchronous Clock Switching Characteristics



Combinatorial Switching Characteristics



Asynchronous Clock Switching Characteristics



XC7336
36 Macrocell CMOS EPLD

Advance Product Information

Features

- Ultra high-performance EPLD
  - 7.5 ns pin-to-pin delay
  - 125 MHz maximum clock frequency
- Incorporates four Fast Function Blocks
- 100% interconnect matrix
- 36 Macrocells with programmable I/O architecture
- 18 outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 44-pin leaded chip carrier package

General Description

The XC7336 is a member of the Xilinx XC7300 EPLD family. It consists of four Fast Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The four Function Blocks in the XC7336 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM. For complete description of device functionality, see the XC7300 EPLD Family data sheet.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

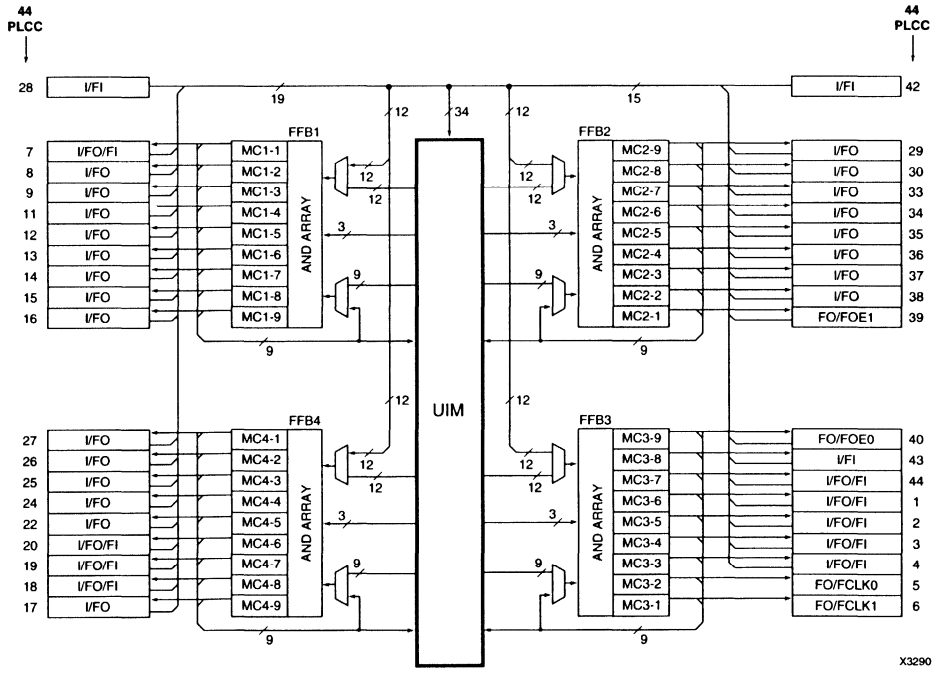


Figure 1. XC7336 Functional Block Diagram

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 4-2.

For a detailed description of the device timing, see pages 4-9 and 4-10.

For component availability and package physical dimensions, see Section 5.

XC7354
54 Macrocell CMOS EPLD

Advance Product Information

Features

- High-Performance EPLD
  - 10 ns pin-to-pin delay
  - 100 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - Four High-Density Function Blocks
- 100% interconnect matrix
- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 35 MHz 16-bit accumulators
- 54 Macrocells with programmable I/O architecture
- Up to 54 inputs programmable as direct, latched, or registered
- 18 outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 44- and 68-pin leaded chip carrier package

General Description

The XC7354 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and ten High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The six Function Blocks in the XC7354 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM. For complete description of device functionality, see the XC7300 EPLD Family data sheet.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

Power Management

The XC7354 power management scheme allows designers to control on-chip power dissipation by configuring individual Macrocells to operate in high-performance or low-power modes of operation. Unused Macrocells are turned off to minimize power dissipation.

Figure 7 in the XC7300 CMOS EPLDFamily data sheet shows typical power requirements for the XC73108 device, assuming all Macrocells are enabled and switching at the indicated clock frequency. The top and bottom curves show the two extreme cases of all Macrocells in high-performance mode, and all Macrocells in low-power mode. Actual chip dissipation will be between the two curves.

Power dissipation for each design can be approximated for specific operating conditions using the following equation.

$$I_{CC} = (MC_{LP} \bullet 1.35\ mA) + (MC_{HP} \bullet 2.5\ mA) + (MC_1 \bullet f_1 \bullet 0.02\ mA/MHz) + \ldots + (MC_n \bullet f_n \bullet 0.02\ mA/MHz)$$

Where:

MC_{LP} = Number of Macrocells in low-power mode

MC_{HP} = Number of Macrocells in high-performance mode

MC_1 = Number of Macrocells operating at frequency f_1 in MHz

MC_n = Number of Macrocell operating at frequency f_n in MHz

Note: Number of Macrocells refers to both Fast Function Block (FFB) and High-Density Function Block (FB) Macrocells.

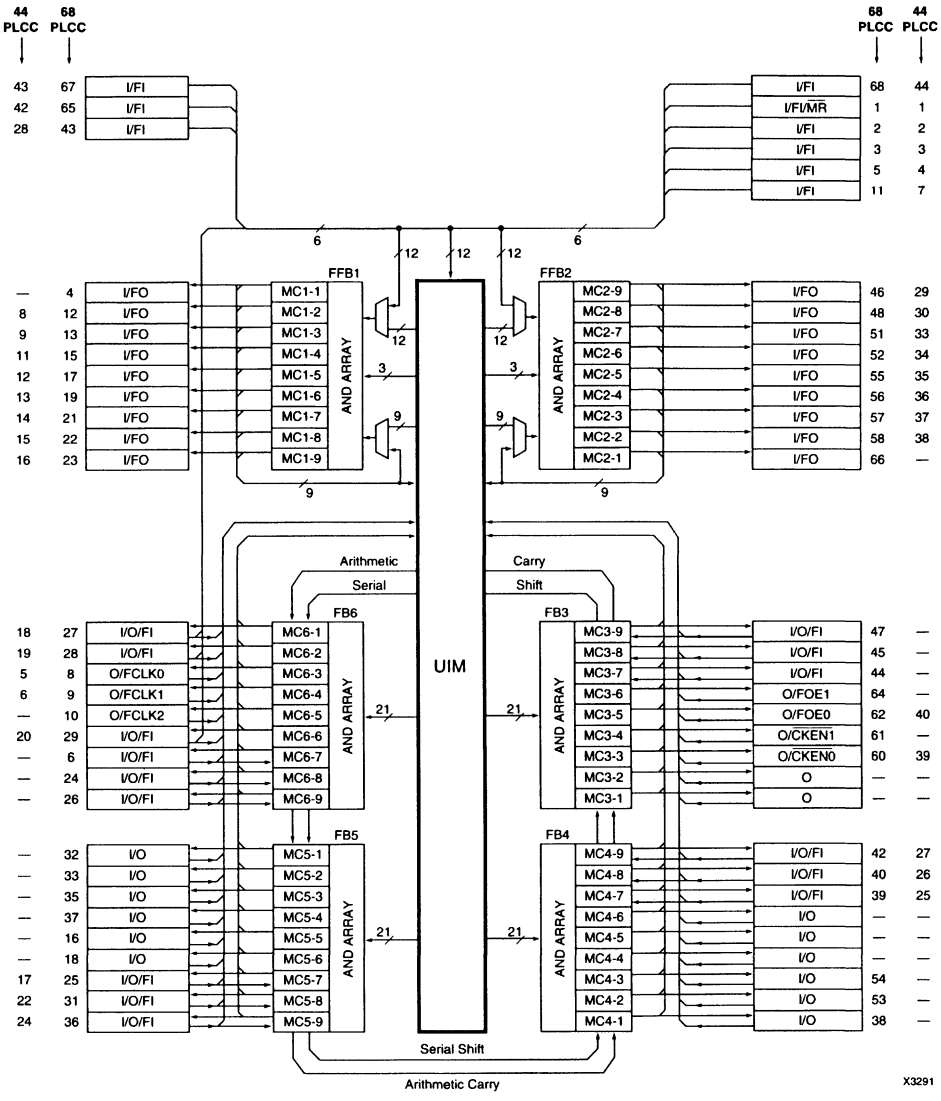


Figure 1. XC7354 Functional Block Diagram

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to 7.0	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to 7.0	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: *Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.*

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND @ 5 V Commercial T_A = 0° C to70° C	4.75	5.25	V
	Supply voltage relative to GND @ 5 V Industrial T_A = -40° C to 85° C	4.5	5.5	V
	Supply voltage relative to GND @ 5 V Military T_C = -55° C to 125° C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND @ 3.3 V	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC}+0.3	V
V_O	Output voltage	0	V_{CCIO}	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I/O = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I/O = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	FO = 24 mA I/O = 12 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I/O = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		10	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance*	V_O = GND f = 1.0 MHz		20	pF

* Sample tested

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{VCCR}	V_{CC} rise time (if MR not used for power-up)**			5	µs
t_{RESET}	Configuration completion time (to outputs operational) following assertion of Master Reset			300	µs

**V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset, and Set inputs must not be asserted until all applicable input and feedback set-up times are met in order to guarantee a predictable initial state.

Fast Function Block (FFB) External AC Characteristics

Symbol	Parameter	XC7354-10 (Coml/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency (1, 2)		100		80		66.7	MHz
t_{SUF}	Fast input setup time before FCLK ↑ (1)	5		6		7		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		ns
t_{COF}	FCLK ↑ to output valid		8.5		9		12	ns
t_{PDFO}	Fast input to output valid (1, 2)		10		12		15	ns
t_{PDFU}	I/O to output valid (1, 2)		16		19		23	ns
t_{CWF}	Fast clock pulse width	5		6		7		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7354-10 (Coml/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	
f_C	Max count frequency (1, 2)		83.3		66.7		55.6	MHz
t_{SU}	I/O setup time before FCLK ↑ (1, 2)	12		15		18		ns
t_H	I/O hold time after FCLK ↑	-4		-5		-6		ns
t_{CO}	FCLK ↑ to output valid		11.5		12		15	ns
t_{PSU}	I/O setup time before p-term clock ↑ (2)	5		7		9		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		18.5		20		24	ns
t_{PD}	I/O to output valid (1, 2)		20		27		32	ns
t_{CW}	Fast clock pulse width	5		6		7		ns
t_{PCW}	P-term clock pulse width	6.5		8		10		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.

2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7354-10 (Coml/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay (2)		1.5		2		2	ns
$t_{FLOGILP}$	Low-power FFB logic array delay (2)		5.5		7		8	ns
t_{FSUI}	FFB register setup time	2.5		3		4		ns
t_{FHI}	FFB register hold time	2.5		3		3		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1		1	ns
t_{FPDI}	FFB register pass through delay		0		1		1	ns
t_{FAOI}	FFB register async. set delay		2.5		3		4	ns
t_{PTXI}	FFB p-term assignment delay		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		5		6.5		8	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7354-10 (Coml/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay (2)		2.5		5		5	ns
t_{LOGILP}	Low power FB logic delay (2)		6.5		9		11	ns
t_{SUI}	FB register setup time	2.5		3		4		ns
t_{HI}	FB register hold time	2.5		4		5		ns
t_{COI}	FB register clock-to-output delay		1		1		1	ns
t_{PDI}	FB register pass through delay		0		4		4	ns
t_{AOI}	FB register async. set/reset delay		3		4		5	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15		18		21		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	10		12		15		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	6		8		9		ns
t_{PCI}	FB p-term clock delay		0		0		0	ns
t_{OEI}	FB p-term output enable delay		4		5		7	ns
t_{CARY8}	ALU carry delay within 1 FB (3)		6		8		12	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block (3)		1.5		2		3	ns

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

3. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

Symbol	Parameter	XC7354-10 (Coml/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) (2)		88.3		66.7		55.6	MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	7		8		10		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		3.5		4		5	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	7		8		10		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	5		6		7		ns
t_{CWLIN}	FCLK pulse width low time	5		6		7		ns

Internal AC Characteristics

Symbol	Parameter	XC7354-10 (Coml/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		3.5		4		5	ns
t_{FOUT}	FFB output buffer and pad delay		5		5		7	ns
t_{OUT}	FB output buffer and pad delay		8		8		10	ns
t_{UIM}	Universal Interconnect Matrix delay		6		7		8	ns
t_{FOEI}	Fast output enable/disable buffer delay		1.0		12		15	ns
t_{FCLKI}	Fast clock buffer delay		2.5		3		4	ns

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

XC7354 Pinouts

68 LCC	44 LCC	Pin Description
1	1	I/FI/ $\overline{MR}$
2	2	I/FI
3	3	I/FI
4	–	I/FO
5	4	I/FI
6	–	I/O/FI
7	–	**GND**
8	5	O/FCLK0
9	6	O/FCLK1
10	–	O/F_{CLK2}
11	7	I/FI
12	8	I/FO
13	9	I/FO
14	10	**GND**
15	11	I/FO
16	–	I/O
17	12	I/FO
18	–	I/O
19	13	I/FO
20	–	V_{CCIO}
21	14	I/FO
22	15	I/FO
23	16	I/FO
24	–	I/O/FI
25	17	I/O/FI
26	–	I/O/FI
27	18	I/O/FI
28	19	I/O/FI
29	20	I/O/FI
30	21	V_{CCINT}
31	22	I/O/FI
32	–	I/O
33	–	I/O
34	23	**GND**

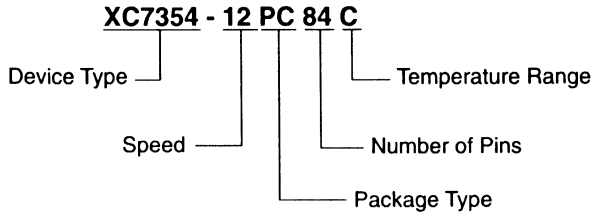
68 LCC	44 LCC	Pin Description
35	–	I/O
36	24	I/O/FI
37	–	I/O
38	–	I/O
39	25	I/O/FI
40	26	I/O/FI
41	–	**GND**
42	27	I/O/FI
43	28	I/FI
44	–	I/O/FI
45	–	I/O/FI
46	29	I/FO
47	–	I/O/FI
48	30	I/FO
49	31	**GND**
50	32	V_{CCIO}
51	33	I/FO
52	34	I/FO
53	–	I/O
54	–	I/O
55	35	I/FO
56	36	I/FO
57	37	I/FO
58	38	I/FO
59	–	V_{CCINT}
60	39	O/$\overline{CKEN0}$
61	–	O/$\overline{CKEN1}$
62	40	O/FOE0
63	41	V_{CCINT}/V_{PP}
64	–	O/FOE1
65	42	I/FI
66	–	I/FO
67	43	I/FI
68	44	I/FI

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family Data Sheet, page 4-2.

For a detailed description of the device timing, see pages 4-9 and 4-10.

For component availability and package physical dimensions, see Section 5.

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commerial and industrial only)

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier
WC44	44-Pin Windowed Ceramic Leaded Chip Carrier
PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C to 125°C (Case)

XC7372
72 Macrocell CMOS EPLD

Advance Product Information

Features

- High-Performance EPLD
  - 10 ns pin-to-pin delay
  - 100 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - Six High-Density Function Blocks
- 100% interconnect matrix
- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 35 MHz 16-bit accumulators
- 72 Macrocells with programmable I/O architecture
- Up to 90 inputs programmable as direct, latched, or registered
- 18 outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 68-, 84-pin leaded chip carrier and 84-pin Pin-Grid-Array packages

General Description

The XC7372 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and six High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The eight Function Blocks in the XC7372 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM. For complete description of device functionality, see the XC7300 EPLD Family data sheet.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

Power Management

The XC7372 power management scheme allows designers to control on-chip power dissipation by configuring individual Macrocells to operate in high-performance or low-power modes of operation. Unused Macrocells are turned off to minimize power dissipation.

Figure 7 in the XC7300 CMOS EPLD Family data sheet shows typical power requirements for the XC73108 device, assuming all Macrocells are enabled and switching at the indicated clock frequency. The top and bottom curves show the two extreme cases of all Macrocells in high-performance mode, and all Macrocells in low-power mode. Actual chip dissipation will be between the two curves.

Power dissipation for each design can be approximated for specific operating conditions using the following equation.

$$I_{CC} = (MC_{LP} \bullet 1.35\ mA) + (MC_{HP} \bullet 2.5\ mA) + (MC_1 \bullet f_1 \bullet 0.02\ mA/MHz) + \ldots + (MC_n \bullet f_n \bullet 0.02\ mA/MHz)$$

Where:

MC_{LP} = Number of Macrocells in low-power mode

MC_{HP} = Number of Macrocells in high-performance mode

MC_1 = Number of Macrocells operating at frequency f_1 in MHz

MC_n = Number of Macrocell operating at frequency f_n in MHz

Note: Number of Macrocells refers to both Fast Function Block (FFB) and High-Density Function Block (FB) Macrocells.

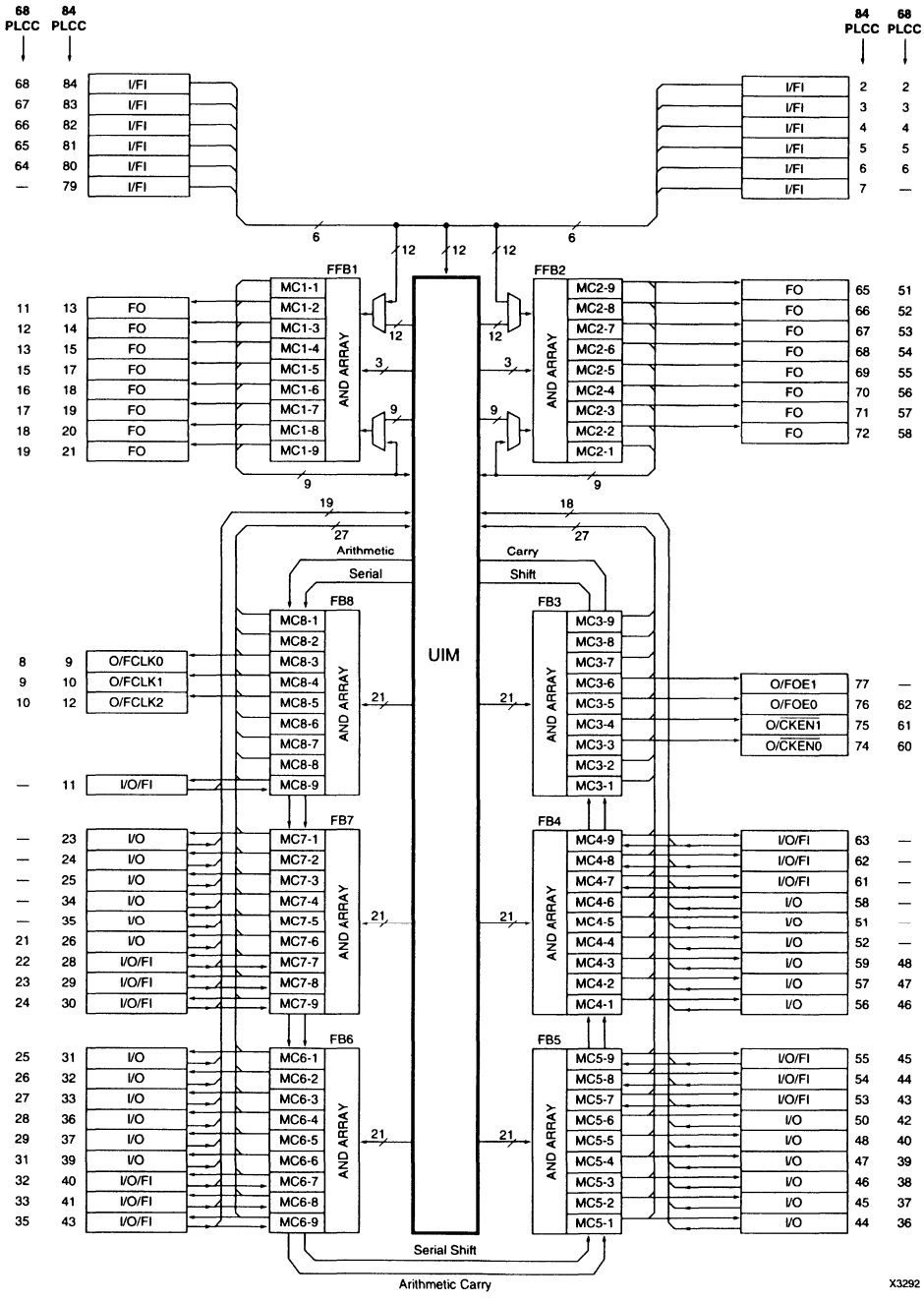


Figure 1. XC7372 Functional Block Diagram

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to 7.0	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to 7.0	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: *Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.*

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND @ 5 V	Commercial t_A = 0° C to70° C	4.75	5.25	V
	Supply voltage relative to GND @ 5 V	Industrial t_A = -40° C to 85° C	4.5	5.5	V
	Supply voltage relative to GND @ 5 V	Military t_C = -55° C to 125° C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND @ 3.3 V		3.0	3.6	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	V_{CC}+0.3	V
V_O	Output voltage		0	V_{CCIO}	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I/O = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I/O = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	FO = 24 mA I/O = 12 mA, V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I/O = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		10	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance*	V_O = GND f = 1.0 MHz		20	pF

* Sample tested

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{VCCR}	V_{CC} rise time (if MR not used for power-up)**			5	µs
t_{RESET}	Configuration completion time (to outputs operational) following assertion of Master Reset			300	µs

**V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset, and Set inputs must not be asserted until all applicable input and feedback set-up times are met in order to guarantee a predictable initial state.

Fast Function Block (FFB) External AC Characteristics

Symbol	Parameter	XC7372-10 (Coml/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency (1, 2)		100		80		66.7	MHz
t_{SUF}	Fast input setup time before FCLK ↑ (1)	5		6		7		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		ns
t_{COF}	FCLK ↑ to output valid		8.5		9		12	ns
t_{PDFO}	Fast input to output valid (1, 2)		10		12		15	ns
t_{PDFU}	I/O to output valid (1, 2)		17		20		25	ns
t_{CWF}	Fast clock pulse width	5		6		7		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7372-10 (Coml/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	
f_C	Max count frequency (1, 2)		71.4		62.5		50	MHz
t_{SU}	I/O setup time before FCLK ↑ (1, 2)	14		16		20		ns
t_H	I/O hold time after FCLK ↑	-5		-6		-8		ns
t_{CO}	FCLK ↑ to output valid		11.5		12		15	ns
t_{PSU}	I/O setup time before p-term clock ↑ (2)	6		7		9		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		19.5		21		26	ns
t_{PD}	I/O to output valid (1, 2)		22		28		34	ns
t_{CW}	Fast clock pulse width	5		6		7		ns
t_{PCW}	P-term clock pulse width	6.5		8		10		ns

Notes:
1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7372-10 (Coml/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay (2)		1.5		2		2	ns
$t_{FLOGILP}$	Low-power FFB logic array delay (2)		5.5		7		8	ns
t_{FSUI}	FFB register setup time	2.5		3		4		ns
t_{FHI}	FFB register hold time	2.5		3		3		ns
t_{FCOI}	FFB register clock-to-output delay		1		1		1	ns
t_{FPDI}	FFB register pass through delay		0		1		1	ns
t_{FAOI}	FFB register async. set delay		2.5		3		4	ns
t_{PTXI}	FFB p-term assignment delay		1		1.2		1.5	ns
t_{FFD}	FFG feeback delay		5		6.5		8.0	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7372-10 (Coml/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay (2)		3.5		4		5	ns
t_{LOGILP}	Low power FB logic delay (2)		7.5		9		11	ns
t_{SUI}	FB register setup time	2.5		3		4		ns
t_{HI}	FB register hold time	3.5		4		5		ns
t_{COI}	FB register clock-to-output delay		1		1		1	ns
t_{PDI}	FB register pass through delay		0		4		4	ns
t_{AOI}	FB register async. set/reset delay		3		4		5	ns
t_{RA}	Set/reset recovery time before FCLK ↑	17		19		23		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	10		12		15		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	6		8		9		ns
t_{PCI}	FB p-term clock delay		0		0		0	ns
t_{OEI}	FB p-term output enable delay		4		5		7	ns
t_{CARY8}	ALU carry delay within 1 FB (3)		6		8		12	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block (3)		1.5		2		3	ns

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

3. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

Symbol	Parameter	XC7372-10 (Coml/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) (2)		71.4		62.5		50	MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	7		8		10		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		3.5		4		5	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	7		8		10		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	5		6		7		ns
t_{CWLIN}	FCLK pulse width low time	5		6		7		ns

Internal AC Characteristics

Symbol	Parameter	XC7372-10 (Coml/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		3.5		4		5	ns
t_{FOUT}	FFB output buffer and pad delay		5		5		7	ns
t_{OUT}	FB output buffer and pad delay		8		8		10	ns
t_{UIM}	Universal Interconnect Matrix delay		7		8		10	ns
t_{FOEI}	Fast output enable/disable buffer delay		10		12		15	ns
t_{FCLKI}	Fast clock buffer delay		2.5		3		4	ns

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

XC7372 Pinouts

84 LCC	68 LCC	Pin Description
1	1	$\overline{MR}$
2	2	I/FI
3	3	I/FI
4	4	I/FI
5	5	I/FI
6	6	I/FI
7	–	I/FI
8	7	**GND**
9	8	O/FCLK0
10	9	O/FCLK1
11	–	I/O/FI
12	10	O/FCLK2
13	11	FO
14	12	FO
15	13	FO
16	14	**GND**
17	15	FO
18	16	FO
19	17	FO
20	18	FO
21	19	FO
22	20	V_{CCIO}
23	–	I/O
24	–	I/O
25	–	I/O
26	21	I/ O
27	–	**GND**
28	22	I/O/FI
29	23	I/OFI
30	24	I/O/FI
31	25	I/O
32	26	I/O
33	27	I/O
34	–	I/O
35	–	I/O
36	28	I/O
37	29	I/O
38	30	V_{CCINT}
39	31	I/O
40	32	I/O/FI
41	33	I/O/FI
42	34	**GND**

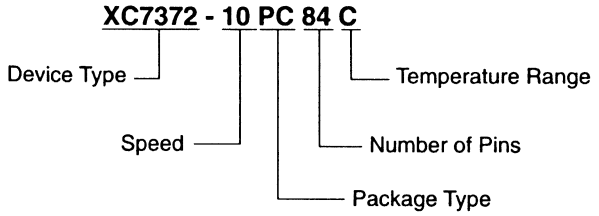
84 LCC	68 LCC	Pin Description
43	35	I/O/FI
44	36	I/O
45	37	I/O
46	38	I/O
47	39	I/O
48	40	I/O
49	41	**GND**
50	42	I/O
51	–	I/O
52	–	I/O
53	43	I/OFI
54	44	I/O/FI
55	45	I/O/FI
56	46	I/O
57	47	I/O
58	–	I/O
59	48	I/O
60	49	**GND**
61	–	I/O/FI
62	–	I/O/FI
63	–	I/O/FI
64	50	V_{CCIO}
65	51	FO
66	52	FO
67	53	FO
68	54	FO
69	55	FO
70	56	FO
71	57	FO
72	58	FO
73	59	V_{CCINT}
74	60	O/$\overline{CKEN0}$
75	61	O/$\overline{CKEN1}$
76	62	O/FOE0
77	–	O/FOE1
78	63	V_{CCINT}/V_{PP}
79	–	I/FFI
80	64	I/FFI
81	65	I/FFI
82	66	I/FFI
83	67	I/FFI
84	68	I/FFI

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 4-2.

For a detailed description of the device timing, see pages 4-9 and 4-10.

For component availability and package physical dimensions, see Section 5.

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)

Packaging Options

PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier
PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PG84	84-Pin Ceramic Pin Grid Array

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C to 125°C (Case)

XC73108
108 Macrocell CMOS EPLD

Preliminary Product Specifidcations

Features

- High-Performance EPLD
  - 12 ns pin-to-pin delay
  - 80 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 10 High-Density Function Blocks
- 100% interconnect matrix
- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 35 MHz 16-bit accumulators
- 108 Macrocells with programmable I/O architecture
- Up to 90 inputs programmable as direct, latched, or registered
- 18 outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 84-pin leaded chip carrier, 144-pin pin-grid-array packages and 160-pin plastic quad flat pack

General Description

The XC73108 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and ten High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The 12 Function Blocks in the XC73108 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM. For complete description of device functionality, see the XC7300 EPLD Family data sheet.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

Power Management

The XC73108 power management scheme allows designers to control on-chip power dissipation by configuring individual Macrocells to operate in high-performance or low-power modes of operation. Unused Macrocells are turned off to minimize power dissipation.

Figure 7 in the XC7300 CMOS EPLD Family data sheet shows typical power requirements for the XC73108 device, assuming all Macrocells are enabled and switching at the indicated clock frequency. The top and bottom curves show the two extreme cases of all Macrocells in high-performance mode, and all Macrocells in low-power mode. Actual chip dissipation will be between the two curves.

Power dissipation for each design can be approximated for specific operating conditions using the following equation.

$$I_{CC} = (MC_{LP} \bullet 1.35\ mA) + (MC_{HP} \bullet 2.5\ mA) + (MC_1 \bullet f_1 \bullet 0.02\ mA/MHz) + \ldots + (MC_n \bullet f_n \bullet 0.02\ mA/MHz)$$

Where:

MC_{LP} = Number of Macrocells in low-power mode

MC_{HP} = Number of Macrocells in high-performance mode

MC_1 = Number of Macrocells operating at frequency f_1 in MHz

MC_n = Number of Macrocell operating at frequency f_n in MHz

Note: Number of Macrocells refers to both Fast Function Block (FFB) and High-Density Function Block (FB) Macrocells.

For example, in a system design with 72 Macrocells in low-power mode at 20 MHz, 18 Macrocells in high-performance mode at 40 MHz, and 18 Macrocells in high-performance mode at 80 MHz:

$$I_{CC} = (72 \bullet 1.35) + (36 \bullet 2.5) + (72 \bullet 20 \bullet 0.02) + (18 \bullet 40 \bullet 0.02) + (18 \bullet 80 \bullet 0.02)$$

$$I_{CC} = 97 + 90 + 29 + 14 + 29 = 259\ mA$$

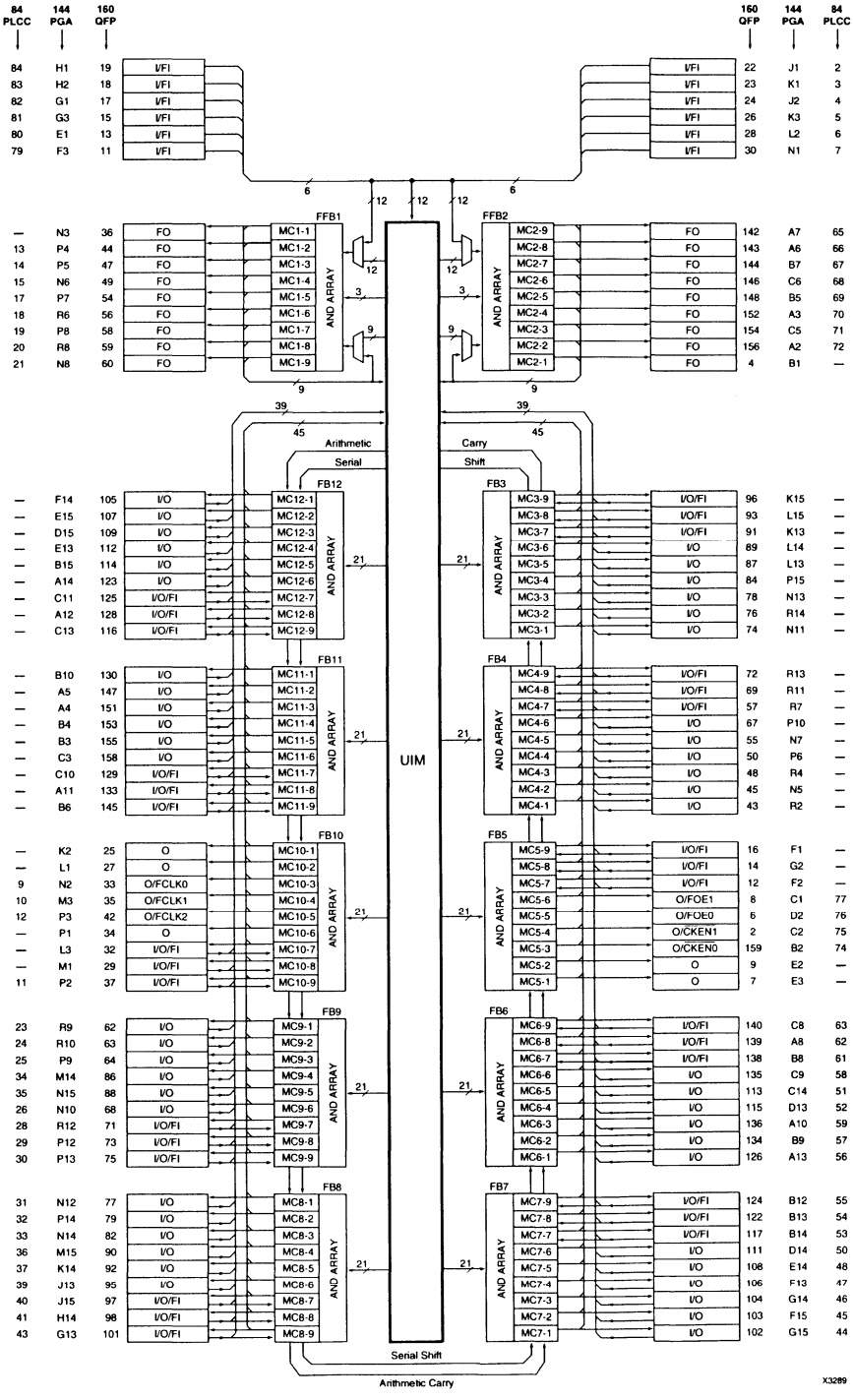


Figure 1. XC73108 Functional Block Diagram

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to 7.0	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to 7.0	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: *Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.*

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND @ 5 V	Commercial t_A = 0° C to70° C	4.75	5.25	V
	Supply voltage relative to GND @ 5 V	Industrial t_A = -40° C to 85° C	4.5	5.5	V
	Supply voltage relative to GND @ 5 V	Military t_C = -55° C to 125° C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND @ 3.3 V		3.0	3.6	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	V_{CC}+0.3	V
V_O	Output voltage		0	V_{CCIO}	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I/O = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I/O = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	FO = 24 mA I/O = 12 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I/O = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		10	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance*	V_O = GND f = 1.0 MHz		20	pF

* Sample tested

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{VCCR}	V_{CC} rise time (if MR not used for power-up)**			5	µs
t_{RESET}	Configuration completion time (to outputs operational) following assertion of Master Reset			300	µs

**V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset, and Set inputs must not be asserted until all applicable input and feedback set-up times are met in order to guarantee a predictable initial state.

Fast Function Block (FFB) External AC Characteristics

Symbol	Parameter	XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency (1, 2)		80		67		50	MHz
t_{SUF}	Fast input setup time before FCLK ↑ (1)	6		7		10		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		ns
t_{COF}	FCLK ↑ to output valid		9		12		15	ns
t_{PDFO}	Fast input to output valid (1, 2)		12		15		20	ns
t_{PDFU}	I/O to output valid (1, 2)		22		27		35	ns
t_{CWF}	Fast clock pulse width	6		7		9		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	
f_C	Max count frequency (1, 2)		55		45		35	MHz
t_{SU}	I/O setup time before FCLK ↑ (1, 2)	18		22		28		ns
t_H	I/O hold time after FCLK ↑	-8		-10		-13		ns
t_{CO}	FCLK ↑ to output valid		12		15		20	ns
t_{PSU}	I/O setup time before p-term clock ↑ (2)	7		9		12		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		23		28		36	ns
t_{PD}	I/O to output valid (1, 2)		30		36		45	ns
t_{CW}	Fast clock pulse width	6		7		9		ns
t_{PCW}	P-term clock pulse width	8		10		12		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.

2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay (2)		2		2		3	ns
$t_{FLOGILP}$	Low-power FFB logic array delay (2)		7		8		11	ns
t_{FSUI}	FFB register setup time	3		4		6		ns
t_{FHI}	FFB register hold time	3		3		4		ns
t_{FCOI}	FFB register clock-to-output delay		1		1		1	ns
t_{FPDI}	FFB register pass through delay		1		1		2	ns
t_{FAOI}	FFB register async. set delay		3		4		6	ns
t_{PTXI}	FFB p-term assignment delay		1.2		1.5		2	ns
t_{FFD}	FFB feedback delay		6.5		8		10	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay (2)		4		5		6	ns
t_{LOGILP}	Low power FB logic delay (2)		9		11		14	ns
t_{SUI}	FB register setup time	3		4		6		ns
t_{HI}	FB register hold time	4		5		6		ns
t_{COI}	FB register clock-to-output delay		1		1		1	ns
t_{PDI}	FB register pass through delay		4		4		4	ns
t_{AOI}	FB register async. set/reset delay		4		5		7	ns
t_{RA}	Set/reset recovery time before FCLK ↑	21		25		31		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	12		15		20		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	8		9		12		ns
t_{PCI}	FB p-term clock delay		0		0		0	ns
t_{OEI}	FB p-term output enable delay		5		7		9	ns
t_{CARY8}	ALU carry delay within 1 FB (3)		8		12		15	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block (3)		2		3		4	ns

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

3. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

Symbol	Parameter	XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) (2)		55		45		35	MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	8		10		12		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		4		5		6	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	8		10		12		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	6		7		9		ns
t_{CWLIN}	FCLK pulse width low time	6		7		9		ns

Internal AC Characteristics

Symbol	Parameter	XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		4		5		6	ns
t_{FOUT}	FFB output buffer and pad delay		5		7		9	ns
t_{OUT}	FB output buffer and pad delay		8		10		14	ns
t_{UIM}	Universal Interconnect Matrix delay		10		12		15	ns
t_{FOEI}	Fast output enable/disable buffer delay		12		15		20	ns
t_{FCLKI}	Fast clock buffer delay		3		4		5	ns

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

XC73108 Pinouts

160 QFP	144 PGA	84 LCC	Pin Description
1	D3	–	V_{CCIO}
2	C2	75	O/$\overline{CKEN1}$
4	B1	–	FO
6	D2	76	O/F_{OE0}
7	E3	–	O
8	C1	77	O/F_{OE1}
9	E2	–	O
10	D1	78	V_{CCINT}/V_{PP}
11	F3	79	I/FI
12	F2	–	I/O/FI
13	E1	80	I/FI
14	G2	–	I/O/FI
15	G3	81	I/FI
16	F1	–	I/O/FI
17	G1	82	I/FI
18	H2	83	I/FI
19	H1	84	I/FI
20	H3	–	**GND**
21	J3	1	MRX
22	J1	2	I/FI
23	K1	3	I/FI
24	J2	4	I/FI
25	K2	–	O
26	K3	5	I/FI
27	L1	-	O
28	L2	6	I/FI
29	M1	–	I/O/FI
30	N1	7	I/FI
31	M2	8	**GND**
32	L3	–	I/O/FI
33	N2	9	O/F_{CLK0}
34	P1	–	O
35	M3	10	O/F_{CLK1}
36	N3	–	FO
37	P2	11	I/O/FI
40	R1	–	**GND**

160 QFP	144 PGA	84 LCC	Pin Description
41	N4	–	V_{CCIO}
42	P3	12	O/F_{CLK2}
43	R2	–	I/O
44	P4	13	FO
45	N5	–	I/O
46	R3	–	V_{CCINT}
47	P5	14	FO
48	R4	–	I/O
49	N6	15	FO
50	P6	–	I/O
51	R5	16	**GND**
54	P7	17	FO
55	N7	–	I/O
56	R6	18	FO
57	R7	–	I/O/FI
58	P8	19	FO
59	R8	20	FO
60	N8	21	FO
61	N9	22	V_{CCIO}
62	R9	23	I/O
63	R10	24	I/O
64	P9	25	I/O
67	P10	–	I/O
68	N10	26	I/O
69	R11	–	I/O/FI
70	P11	27	**GND**
71	R12	28	I/O/FI
72	R13	–	I/O/FI
73	P12	29	I/O/FI
74	N11	–	I/O
75	P13	30	I/O/FI
76	R14	–	I/O
77	N12	31	I/O
78	N13	–	I/O
79	P14	32	I/O
80	R15	–	**GND**

XC73108 Pinouts (continued)

160 QFP	144 PGA	84 LCC	Pin Description
81	M13	–	V_{CCIO}
82	N14	33	I/O
84	P15	–	I/O
86	M14	34	I/O
87	L13	–	I/O
88	N15	35	I/O
89	L14	–	I/O
90	M15	36	I/O
91	K13	–	I/O/FI
92	K14	37	I/O
93	L15	–	I/O/FI
94	J14	38	V_{CCINT}
95	J13	39	I/O
96	K15	–	I/O/FI
97	J15	40	I/O/FI
98	H14	41	I/O/FI
99	H15	–	**GND**
100	H13	42	**GND**
101	G13	43	I/O/FI
102	G15	44	I/O
103	F15	45	I/O
104	G14	46	I/O
105	F14	–	I/O
106	F13	47	I/O
107	E15	–	I/O
108	E14	48	I/O
109	D15	–	I/O
110	C15	49	**GND**
111	D14	50	I/O
112	E13	–	I/O
113	C14	51	I/O
114	B15	–	I/O
115	D13	52	I/O
116	C13	–	I/O/FI
117	B14	53	I/O/FI
120	A15	–	**GND**

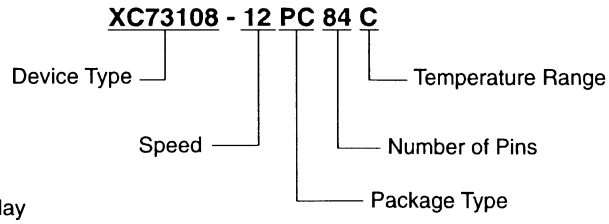
160 QFP	144 PGA	84 LCC	Pin Description
121	C12	–	V_{CCIO}
122	B13	54	I/O/FI
123	A14	–	I/O
124	B12	55	I/O/FI
125	C11	–	I/O/FI
126	A13	56	I/O
127	B11	–	**GND**
128	A12	–	I/O/FI
129	C10	–	I/O/FI
130	B10	–	I/O
133	A11	–	I/O/FI
134	B9	57	I/O
135	C9	58	I/O
136	A10	59	I/O
137	A9	60	**GND**
138	B8	61	I/O/FI
139	A8	62	I/O/FI
140	C8	63	I/O/FI
141	C7	64	V_{CCIO}
142	A7	65	FO
143	A6	66	FO
144	B7	67	FO
145	B6	–	I/O/FI
146	C6	68	FO
147	A5	–	I/O
148	B5	69	FO
151	A4	–	I/O
152	A3	70	FO
153	B4	–	I/O
154	C5	71	FO
155	B3	–	I/O
156	A2	72	FO
157	C4	73	V_{CCINT}
158	C3	–	I/O
159	B2	74	O/$\overline{\text{CKEN0}}$
160	A1	–	**GND**

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 4-2.

For a detailed description of the device timing, see pages 4-9 and 4-10.

For component availability and package physical dimensions, see Section 5.

Ordering Information



Speed Options

-20	20 ns pin-to-pin delay
-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay (commercial and industrial only)

Packaging Options

PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PG144	144-Pin Windowed Pin-Grid-Array
PQ160	160-Pin Plastic Quad Flat Pack

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C to 125°C (Case)

XC73144
144 Macrocell CMOS EPLD

Advance Product Information

Features

- High-Performance EPLD
  - 10 ns pin-to-pin delay
  - 100 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 14 High-Density Function Blocks
- 100% interconnect matrix
- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 35 MHz 16-bit accumulators
- 144 Macrocells with programmable I/O architecture
- Up to 90 inputs programmable as direct, latched, or registered
- 18 outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 184-pin pin-grid-array package

General Description

The XC73144 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and 14 High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The 16 Function Blocks in the XC73144 are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM. For complete description of device functionality, see the XC7300 EPLD Family data sheet.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 4-2.

For a detailed description of the device timing, see pages 4-9 and 4-10.

For component availability and package physical dimensions, see Section 5.

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SECTION 5

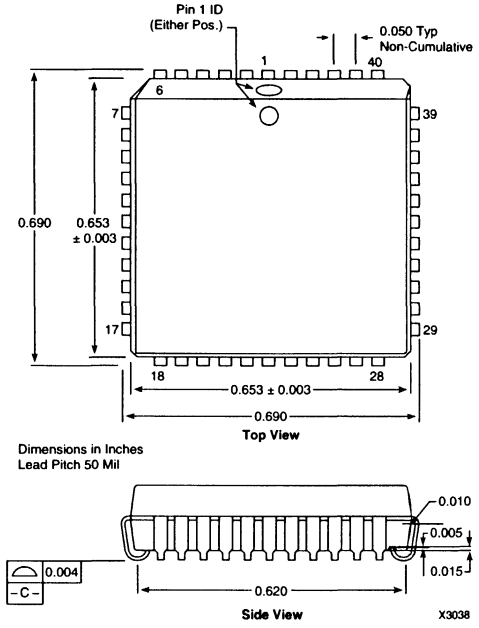
Component Availability

XC7000 Family Package Selection Chart

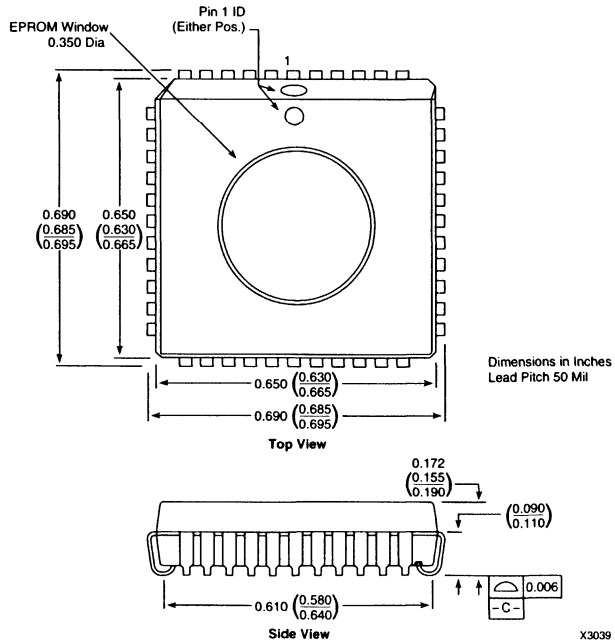
PINS		44		68		84			144	160	184
TYPE		PLAST PLCC	CERAM CLCC	PLAST PLCC	CERAM CLCC	PLAST PLCC	CERAM CLCC	CERAM PGA	CERAM PGA	PLAST PQFP	CERAM PGA
CODE		PC44	WC44	PC68	WC68	PC84	WC84	PG84	PG144	PQ160	PG184
XC7236	-30	CI	CI								
	-25	CI	CI								
XC7236A	-25	CI	CI(M)								
	-20	CI	CI(M)								
	-16	CI	CI								
XC7272	-30			CI	CI	CI	CI	CI			
	-25			CI	CI	CI	CI	CI			
XC7272A	-25			CI	CI	CI	CI(M)	(CI)			
	-20			CI	CI	CI	CI(M)	(CI)			
	-16			CI	CI	CI	CI(M)	(CI)			
XC7336		(CI)	(CIM)								
XC7354	-15	CI	CI	CI	CI(M)						
	-12	CI	CI	CI	CI(M)						
	-10	CI	CI	CI	CI						
XC7372	-15			(CI)	(CI)	(CI)	(CIM)	(CI)			
	-12			(CI)	(CI)	(CI)	(CIM)	(CI)			
	-10			(CI)	(CI)	(CI)	(CI)	(CI)			
XC73108	-20					CI	CI		CI(M)	CI	
	-15					CI	CI		CI(M)	CI	
	-12					CI	CI		CI	CI	
XC73144											(CIM)

C = Commercial = 0°C to + 70°C I = Industrial = -40°C to + 85°C M = Military = -55°C to 125°C Parenthesis indicate future product plans

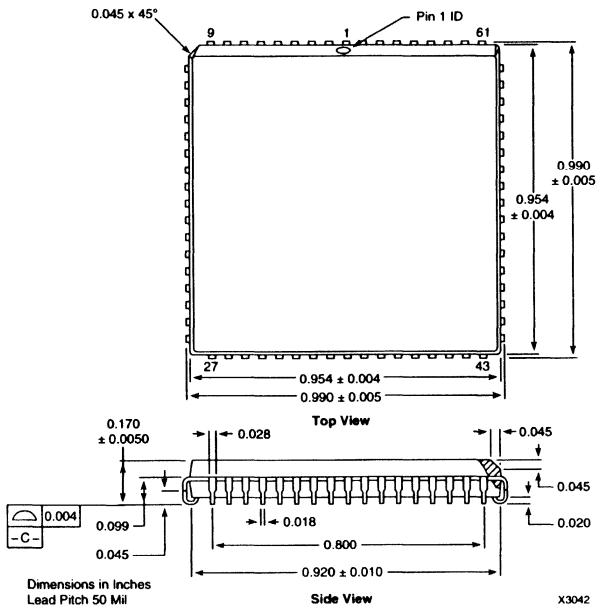
X3322



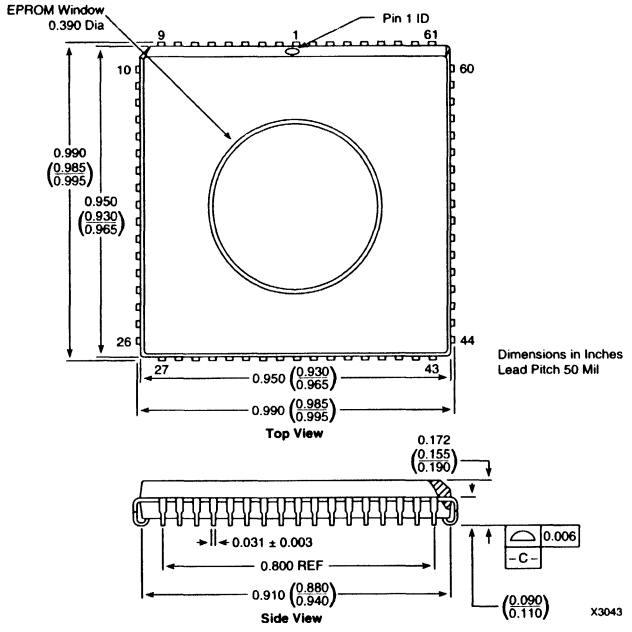
44-Pin Plastic PLCC (PC44)



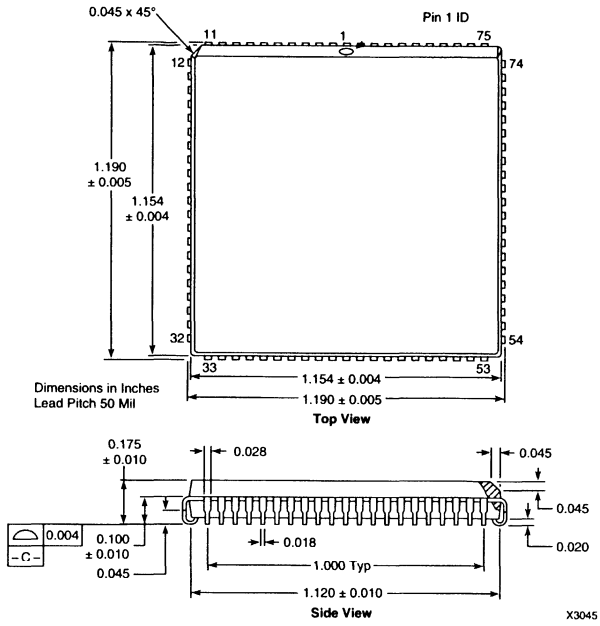
44-Pin Windowed Ceramic CLCC (WC44)



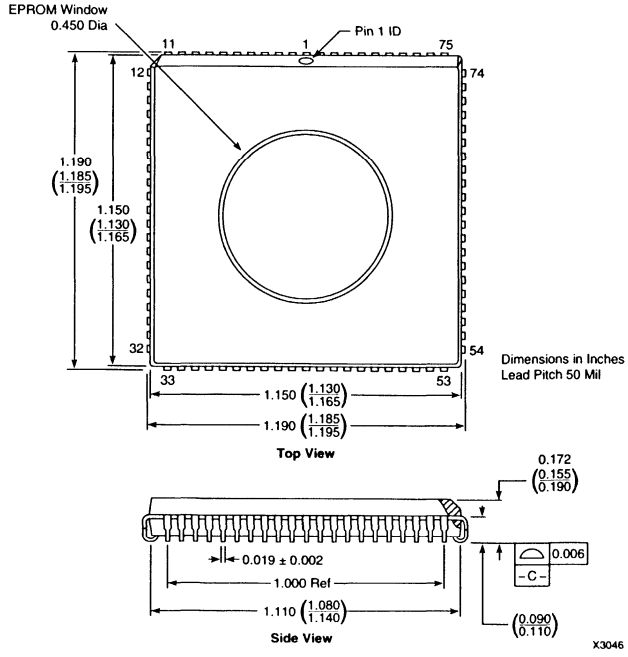
68-Pin Plastic PLCC (PC68)



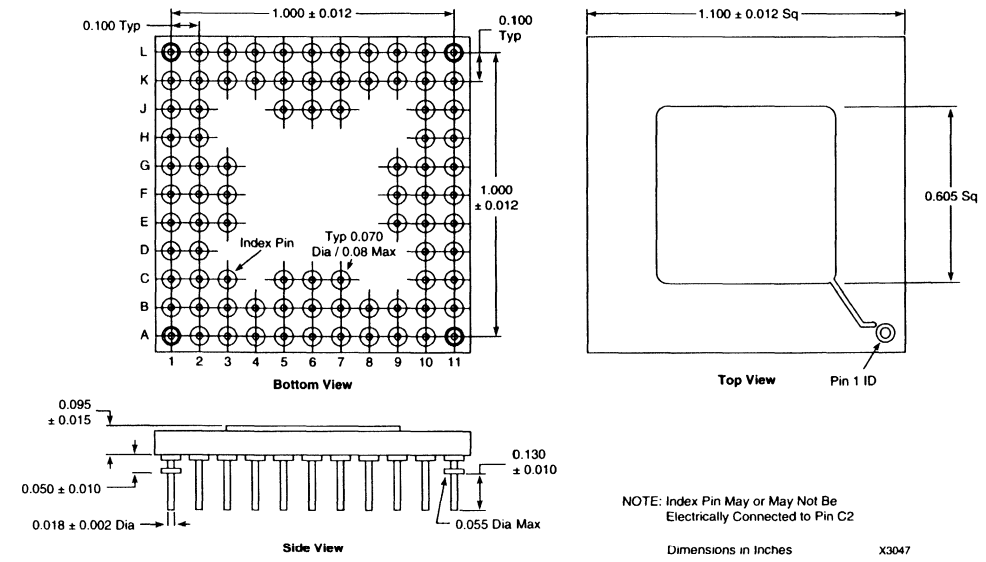
68-Pin Windowed CLCC (WC68)



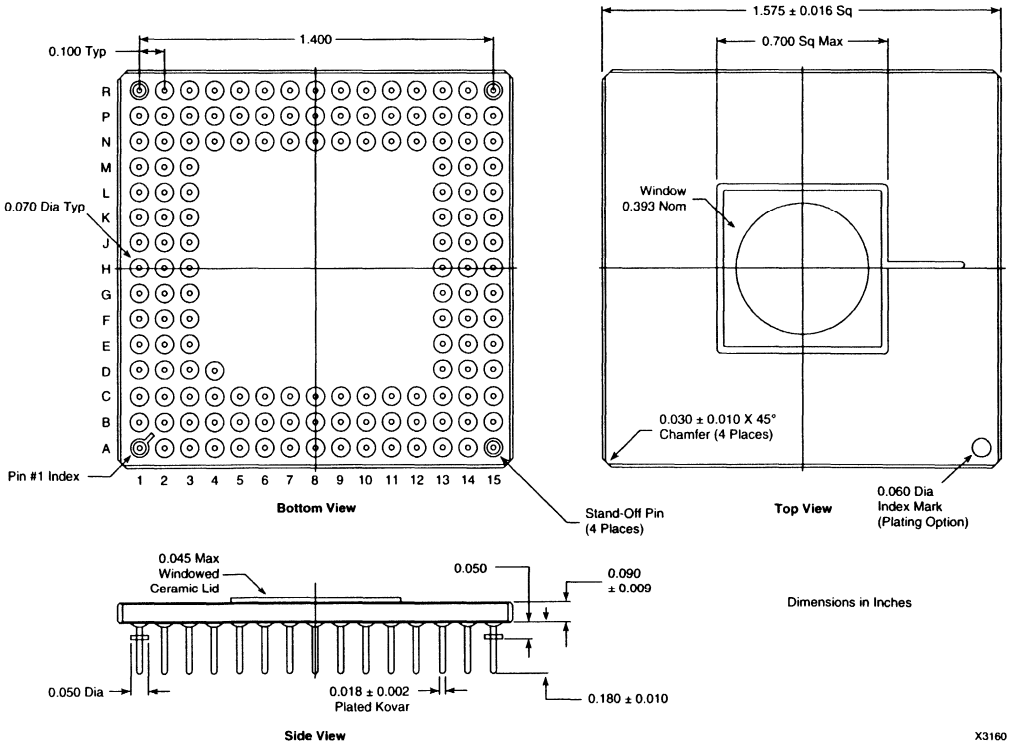
84-Pin Plastic PLCC (PC84)



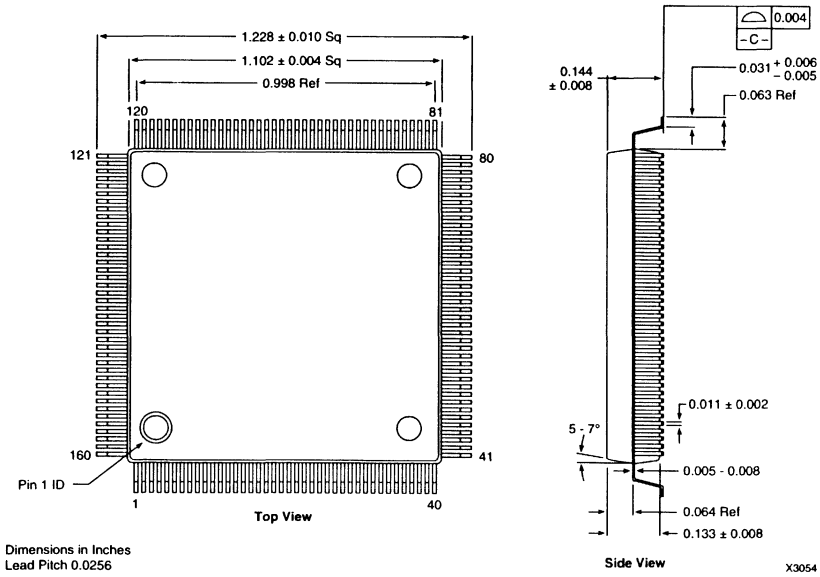
84-Pin Windowed CLCC (WC84)



84-Pin Ceramic PGA (PG84)



144-Pin Ceramic PGA (PG144)



160-Pin Plastic PQFP (PQ160)

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SECTION 6

Using ABEL to Design with Xilinx EPLDs

BY JEFFREY GOLDBERG

Introduction

When it comes to programmable logic, silicon is only part of the solution. Software is required to translate ideas into reality. The Xilinx EPLD Translator (XEPLD) is the Xilinx EPLD software solution. Operating under the Xilinx XACT Design Manager (XDM), XEPLD is designed to work with familiar industry standard front end design tools. In addition to interfacing to schematic capture tools, XEPLD also works with industry standard PAL logic compilers and languages such as ABEL, CUPL and PALASM. Once the design is entered, XEPLD simply acts as a fitter, taking the design description and automatically partitioning the logic, then mapping it into the chosen Xilinx EPLD.

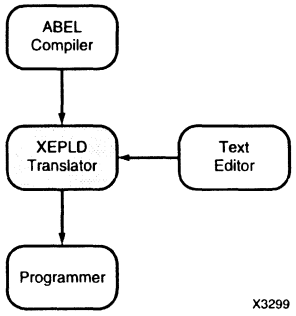

Figure 1. Development System Overview

Most logic compilers generate a PALASM Boolean equation file that can be read by XEPLD. ABEL however, also generates PLUSASM, the XEPLD native syntax. This allows designers to take advantage of PLUSASM expressions that target specific resources of these devices. Once the PLUSASM file is generated, a text editor is used to create a top level design file. Since this file need only contain declaration statements that manage the design (e.g. define the chip's inputs and outputs) it is created with a minimum of effort.

This application note illustrates the design flow for using ABEL to design with Xilinx EPLDs. ABEL-HDL language constructs that generate the most efficient PLUSASM equations are identified. Finally, techniques allowing the user to take advantage of the Xilinx EPLD input pad registers and the UIM ANDing capability are demonstrated.

ABEL Design Flow

The ABEL design flow is illustrated in Figure 2. Using ABEL, the design is compiled, then optimized using REDUCE BY PIN - AUTO POLARITY (This option yields the best results for Xilinx EPLDs). PLUSASM is then selected from the ABEL XFER menu to generate the PLUSASM equation file, <filename>.pld.

The ABEL source code should contain a DEVICE statement, although a specific device need not be targeted when the design is compiled. This causes ABEL to place the required CHIP statement in the resulting PLUSASM file.

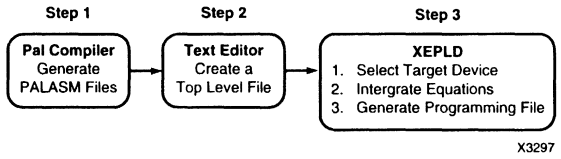

Figure 2. Development System Overview

The top level design file is written with a text editor. XEPLD reads this top level design file, concatenates the equations contained in the ABEL generated PLUSASM file and maps the design into the chosen Xilinx EPLD. A sample design file is shown in Figure 3. This design file, PORT_4.PLD, was created for a Quad Ported Memory Controller, (See the Xilinx EPLD data book for the detailed application note). This file is written in PLUSASM and contains keywords that target architectural features of the Xilinx EPLD (e.g. input registers and UIM logic), but should look very familiar to those familiar with PALASM.

Like PALASM, this file begins with a title block for design documentation, followed by INCLUDE_EQN keywords that instruct XEPLD to concatenate the PLUSASM equations contained in the three included files that were generated by the ABEL compiler for this design.

The CHIP statement contains the filename of the top level file (without the file extension) and targets a Xilinx EPLD.

INPUTPIN, OUTPUTPIN and NODE keywords then follow to define the devices inputs, outputs and nodes. This is followed by the FASTCLOCK keyword that assigns signals to the global FastClock lines.

The EQUATIONS keyword indicates where the equations section of the design file begins. After reading this keyword, XEPLD reads all of the equations in the included files.

After completing the top level design file, invoke the Xilinx Design Manager and do the following:

- Select the target device:

  Open up the FAMILY menu and select the XC7000 device family. Then open up the PART menu and select the target Xilinx EPLD.

- Integrate the equations:

  Open up the FITTER menu and select FITEQN, then PORT_4.PLD. XEPLD then processes the design to create the database file PORT_4.VMH.

- Generate the device programming file:

  Open up the VERIFY menu and select MAKEPRG, then PORT_4.VMH. Assign the signature, PORT4.A, and XEPLD will now produce the device programming file, PORT_4.PRG.

The device can now be programmed and the correct system operation verified.

```
TITLE           Quad-Ported Memory Controller
AUTHOR          Jeffrey Goldberg
COMPANY         Xilinx
DATE            02/26/93

INCLUDE_EQN 'DRC.PLD'
INCLUDE_EQN 'ARBITER.PLD'
INCLUDE_EQN 'REFRESH.PLD'

CHIP PORT_4 XEPLD
INPUTPIN (RCLK=CLK)   RESET
                      PORT_A_REQ PORT_B_REQ PORT_C_REQ PORT_D_REQ
                      PORT_A_LOCK PORT_B_LOCK PORT_C_LOCK PORT_D_LOCK
                      WRITE BYTE0 BYTE1 BYTE2 BYTE3 BURST

OUTPUTPIN             CAS0 CAS1 CAS2 CAS3 CLR_RFRQ COLUMN_ADDRESS
                      GRANT_A GRANT_B GRANT_C GRANT_D
                      RAS READY RFRQ WE

NODE                  ACCESS_REQ DONE DRAM0 DRAM1 DRAM2 DRAM3 ARB0 ARB1 ARB2
                      QA QB QC QD QE QF QG QH QI QJ

NODE (UIM)            RESTART

FASTCLOCK             CLK

EQUATIONS
```

Figure 3. Top-Level Design File

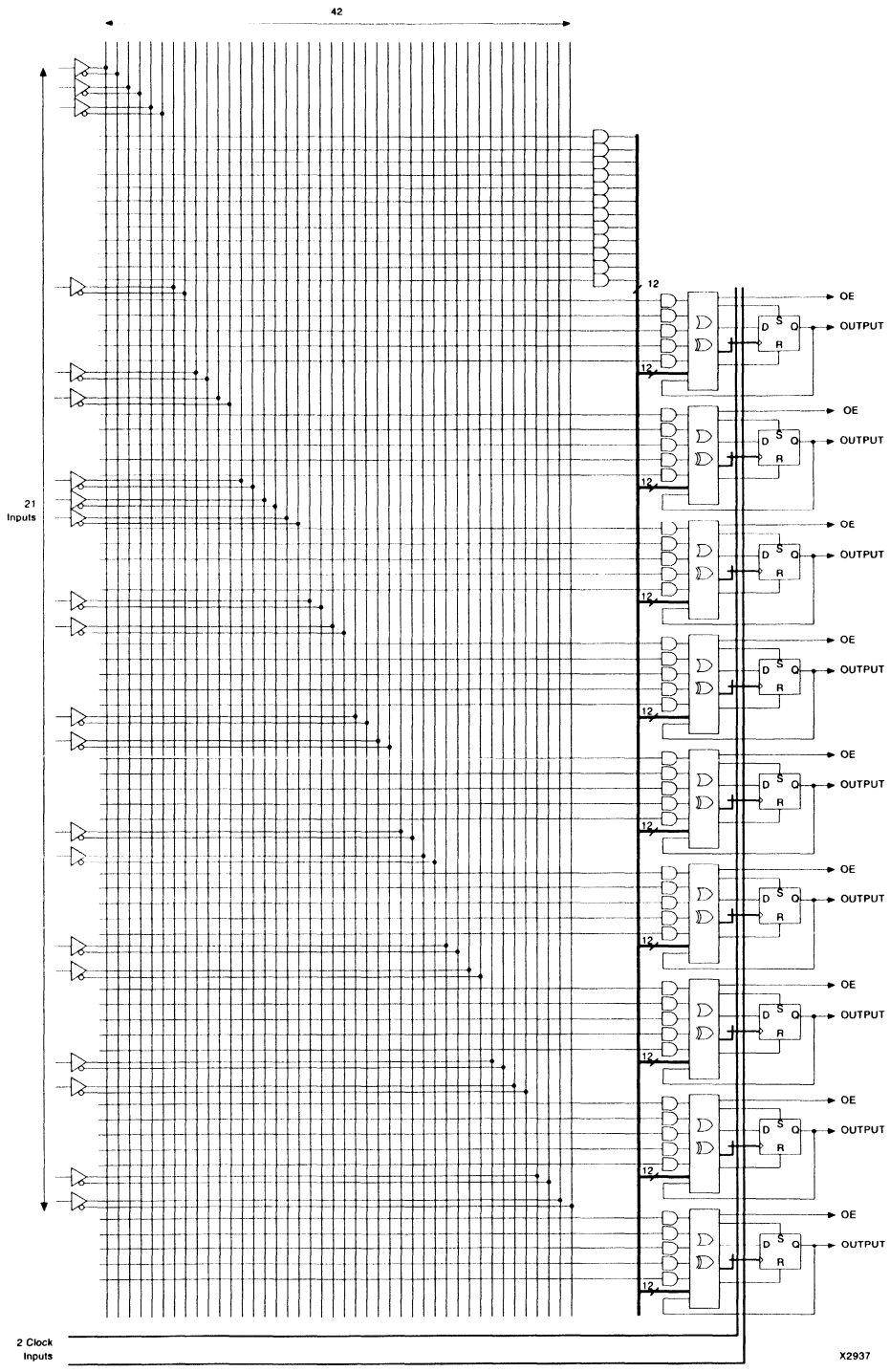

Figure 4. Xilinx EPLD High Density Function Block

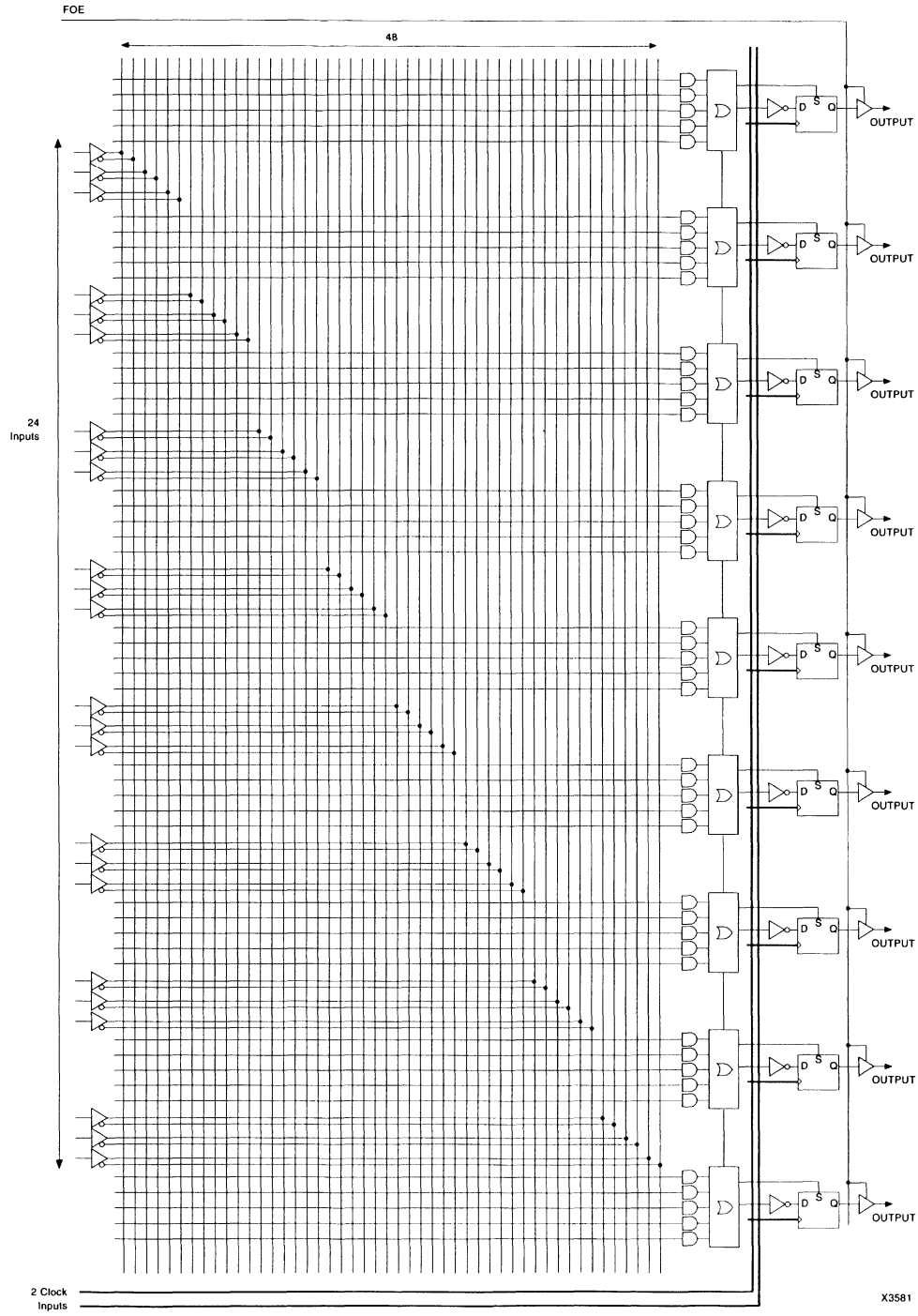

Figure 5. Xilinx EPLD Fast Function Block

Xilinx EPLD Architecture

In order to understand which ABEL-HDL language constructs generate the most efficient PLUSASM code, the reader should have a rudimentary understanding of the Xilinx EPLD architecture. Each device consists of several PAL-like logic blocks, called Function Blocks (FBs), all interconnected by a fully populated switch matrix. Each High Density FB can be thought of as a 21V9 PAL, with 21 complementary inputs and 9 macrocells.

The High Density FB has 5 individual product terms per macrocell. In addition, there are 12 product terms that are shared between all 9 macrocells. Each macrocell can be configured as either registered or combinatorial. Each register has individual set, reset and output enable control and can be clocked either individually or by global clocks. In addition, each macrocell contains an available XOR gate that can be used for XOR functions or toggle flip flop emulation.

In addition to the High Density Function Blocks, each Xilinx XC7300 device contains Fast Function Blocks. These FBs are optimized for speed, and are architecturally different from the High Density FB. Each Fast FB can be thought of as a 24V9 PAL, with 24 complementary inputs and 9 outputs.

Like the High Density FB, there are 5 individual product terms per macrocell and each macrocell can be configured as registered or combinatorial. However, the macrocell is simplified to improve performance. The macrocell output has fixed output inversion (for high speed address decoders), no available XOR gate and may only be clocked by global clocks. The High Density Function Block shared product terms are also eliminated in favor of a higher performance product-term assignment function.

All of the Function Blocks on a Xilinx EPLD are interconnected by a fully populated Universal Interconnect Matrix (UIM).

In addition to serving as an interconnect, the structure of the UIM allows it to function as very wide input WIRED - AND array. This allows the EPLD to generate product terms in the UIM - just like a low density PAL AND array. And like a PAL, propagation delay is fixed regardless of the number of signals used to generate the product term, or the source and destination of those signals.

Xilinx EPLDs also have programmable I/O blocks for driving the device pins. The I/O blocks can be used to decouple the Function Block outputs from the device pins so the Function Blocks may be buried while still retaining the use of the pin as a device input. The I/O blocks also provide output inversion control and the ability to latch and register input signals.

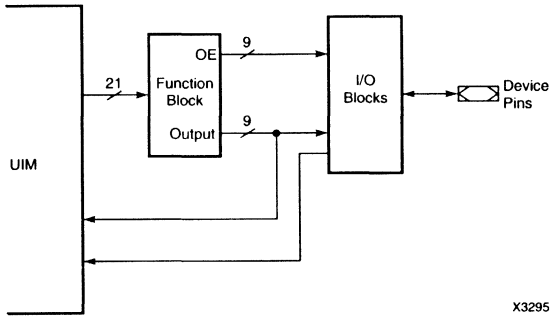

Figure 7. I/O Block

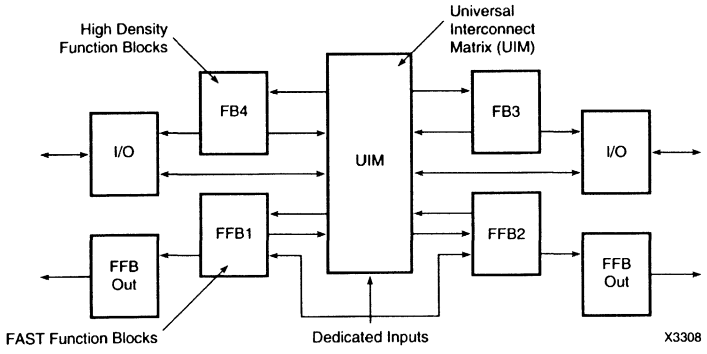

Figure 6. XC7300 Dual Block Architecture

Optimal ABEL-HDL Language Constructs For Xilinx EPLDS

The ABEL PLUSASM writer is capable of targeting the XOR gate available in each High Density Function Block macrocell. This is particularly useful when one wishes to emulate a T flip flop for counter implementations. Instead of declaring the function as a toggle flip flop, the ABEL ISTYPE 'REG,XOR' statement for the node or pin declaration should be used as shown in Figure 8. Then the ABEL XOR_FACTORS keyword is used to define one input of the XOR gate. (See the 1993 Xilinx Databook for details on describing long counters for Xilinx EPLDs with ABEL)

The ABEL dot extensions supported by the ABEL PLUSASM writer are illustrated in Figure 9. Although both the Xilinx EPLD architecture and PLUSASM support dual feedback (separate feedback paths for the macrocell output and I/O pin input) to the UIM, the ABEL PLUSASM writer doesn't. The ABEL PLUSASM writer treats all feedback as coming directly from the macrocell output. PLUSASM declaration statements in the top level design file can relocate the feedback to the I/O pin without any modification to the ABEL generated PLUSASM equations. Alternatively, the equations can be edited with a text editor to take advantage of the dual feedback capability.

```
module refresh
title     'Refresh timer for DRAM controller
          Equation file for XC7236 behavioral-based application example
          Jeffrey Goldberg
          Xilinx';

refresh device;

" Inputs
Clk             pin;
clr_rfrq        pin;                    " low active clear refresh request flag

" Outputs

qj,qi,qh,qg,qf,qe,qd,qc,qb,qa   pin istype 'reg,xor';   " counter bits
restart                         pin istype 'com';       " restart counter start from 0
rfrq                            pin istype 'reg';       " refresh request flag

" Variables

count = [qj,qi,qh,qg,qf,qe,qd,qc,qb,qa];

xor_factors count := count & !restart;                  " q.D2 = q & !restart

equations

restart = (count == 937);                               " restart counter every 15 microseconds

count := (count + 1) & !restart;                        " count up

rfrq := restart                                         " set refresh request flag
     # rfrq & clr_rfrq;                                 " flag remains set until clr_rfrq goes low

 end
```

Figure 8. REFRESH.PLD

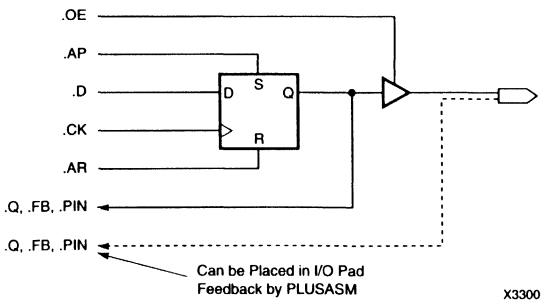

Figure 9. ABEL Dot Extension

Targeting the Xilinx EPLD Input Pad Registers

Xilinx EPLDs contain input pad registers that can be used for input signal synchronization, parameter storage and signal pipelining. Since functions mapped into these registers do not consume macrocell resources, increased logic density is achieved when these registers are utilized.

The ABEL file shown in Figure 10 can be used to synchronize an input signal with a global clock. The ABEL PLUSASM writer will generate PLUSASM equations however, that would map the synchronization register into a macrocell register, not an input pad register.

In order to target an input pad register, there is no need to create an internal node in the ABEL file. Declare the output signal of the input pad register as an input pin in the ABEL source code as shown in Figure 12. Then declare the input pin as a registered input in the top level PLUSASM file with the declaration INPUTPIN (RCLK=clock_signal_name), as shown in Figure 3. The logic will then be mapped into the Xilinx EPLD as shown in Figure 13.

Targeting the Xilinx EPLD UIM

It's easy to map ABEL generated equations into the UIM without any modifications to the ABEL source code or the ABEL generated PLUSASM code. Combinatorial node equations that consist of only a single product term can be mapped into the UIM, instead of consuming Function Block resources (see the XEPLD documentation for details on UIM optimization).

The RESTART equation in the ABEL file shown in Figure 8 generates a single product term. If mapped into a macrocell, the counter outputs would make an extra pass through the chip to generate RESTART, adversely affecting both density and performance. Treating RESTART as a variable in the ABEL code would eliminate the second pass though the chip but would consume 9 of the Function Block's shared product terms when complemented. Instead, use the NODE (UIM) declaration in the top level PLUSASM design file, as shown in Figure 3 for RESTART, to map the function into the UIM.

```
" Inputs
Clk                 pin;
Port_A_Req_Pin      pin;                " Port_A access request strobe

" Nodes
Port_A_Req          node istype 'reg';  " Synchronized Port_A access request strobe

" Outputs
Access_Req          pin istype 'reg';   " Memory arbiter access request strobe

Equations
Port_A_Req := Port_A_Req_Pin;
Access_Req := Port_A_Req & ... # ...;
```

Figure 10. ABEL Code for Signal Synchronization with a Macrocell Register

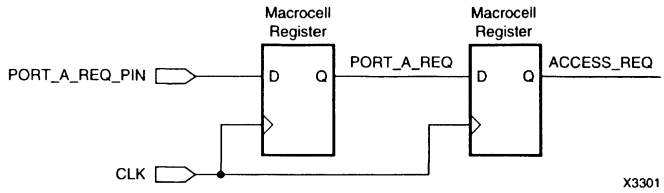

Figure 11. Signal Synchronization with Macrocell Register

```
" Inputs
Clk                 pin;
Port_A_Req          pin;                " Port_A access request strobe

" Outputs
Access_Req          pin istype 'reg';   " Memory arbiter access request strobe

Equations
Access_Req := Port_A_Req & ... # ...;
```

Figure 12. ABEL Source Code for Xilinx EPLD Input Pad Register

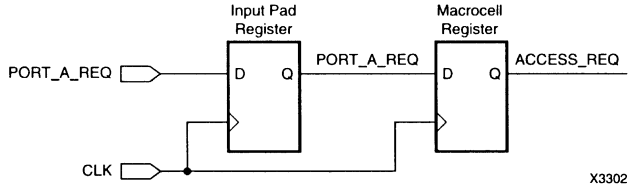

Figure 13. Signal Synchronization with Input Pad Register

Targeting XC7300 Fast Function Blocks

Functions targeted for the 7300 Fast Function Blocks are declared ISTYPE 'NEG'. This declaration instructs ABEL to produce the negative polarity equations required by XEPLD 4.0 for the Fast Function Blocks. Since this declaration is ignored if the ABEL Auto Polarity option is chosen, the REDUCE BY PIN - FIXED option should be selected to insure that the negative polarity equation is produced by the ABEL PLUSASM writer. Statements in the top level PLUSASM design file then instruct XEPLD to map high speed logic into the Fast Function Blocks (See the XEPLD 4.0 documentation for complete details on using the Fast Function Blocks).

Conclusion

ABEL-HDL is a familiar industry standard PAL compiler that can be used to target Xilinx EPLDs directly, and the resulting PLUSASM code can be efficiently mapped by the XEPLD software. Just as with the more familiar 22V10 low-density PAL device, only minimal knowledge of the Xilinx EPLD architecture is required when generating the source code. This combination of a familiar front end design tool (ABEL) and powerful fitter software (XEPLD) allow users to quickly and easily implement dense high performance designs that take full advantage of the Xilinx EPLD architecture.

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- Cost effective way to get started with programmable logic.
- Wide variety of device support – from XC7200 and XC7300 EPLDs to XC2000, XC3000 and XC3100 FPGAs (up to XC3130).
- Includes interfaces to OrCAD or Viewlogic schematic capture and simulation tools

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The Base Development System processes schematic designs from OrCAD or Viewlogic, down to a bitmap ready to be programmed into an EPLD part. Programming is supported by third-party programmer vendors like Data I/O, and by the low-cost Xilinx HW-120 programmer. EPLD designs can also incorporate PALASM-compatible equation files, which are accessible from popular PLD compilers such as Data I/O's ABEL and Logical Device's CUPL.

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The software includes everything you need to compile an OrCAD or Viewlogic design – down to a programmed part. Xilinx's incremental FPGA design methodology allows you to make design changes quickly and easily, without going back to the drawing board. Performance analysis is made easy with the XDelay static timing calculator. The XChecker software and the parallel download cable let you configure parts directly from your PC. Included are a demo board (that works with either XC2000, XC3000 or XC3100 Family FPGAs) and two actual devices.

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XC7272A	✔				✔	✔
XC73108	✔	✔			✔	✔
FPGAs:						
XC2018	✔		✔		✔	
XC2064	✔	✔		✔	✔	
XC3020	✔	✔	✔		✔	
XC3030	✔	✔			✔	
XC3120	✔	✔		✔	✔	
XC3130	✔	✔		✔	✔	

Product Matrix

	Base Development System		
	OrCAD	**Viewlogic**	**Stand-alone (S)**
Schematic Capture			✔
Simulator			✔
Library + Interface	✔	✔	✔
Demo Board	✔	✔	✔
Parallel Down Load Cable	✔	✔	✔
Static Timing Analysis	✔	✔	✔
Sample FPGAs	✔	✔	✔

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Base Development System Software:

DS-OR-BAS-PC1	Including OrCAD interface and libraries
DS-VL-BAS-PC1	Including Viewlogic interface and libraries
DS-VLS-BAS-PC1	Stand-alone version including Viewdraw-LCA, Viewsim-LCA and Viewlogic interface and libraries

Additional Options:

HW-120	Xilinx EPLD Programmer
HW-112	Xilinx Serial PROM Programmer
DS-371-PC1	Xilinx-ABEL

Hardware Requirements:

386 PC or PC-compatible with 8 MB memory and 30 MB disk space.

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